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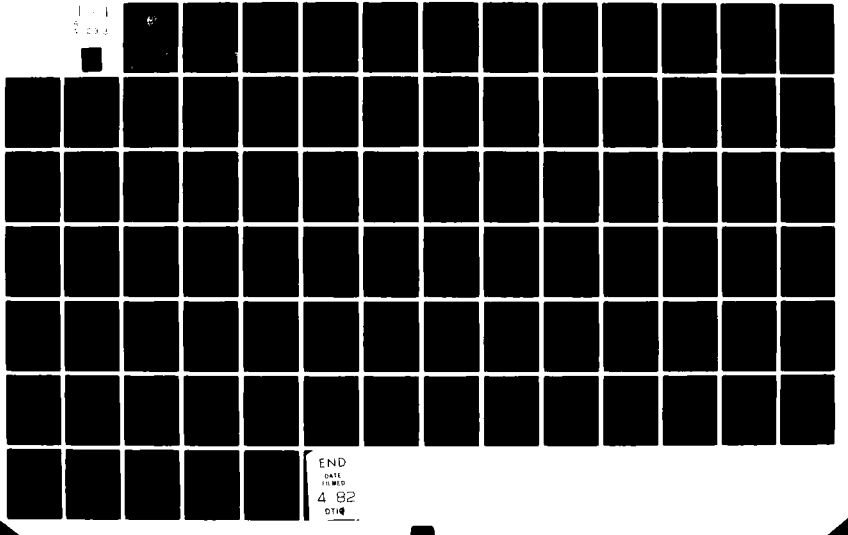

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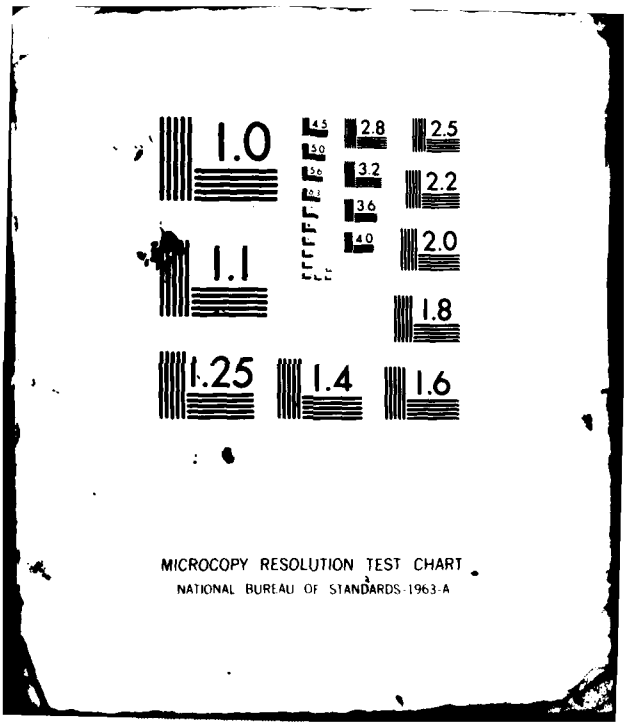
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DEVELOPMENT OF A SURFACE TECHNOLOGY FOR GaAs DEVICES

FINAL TECHNICAL REPORT

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DEZEMBER 1981

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ABSTRACT

The method of two-step anodisation was investigated further. It was found that inversion-type capacitance increases can also be obtained occasionally by anodizing an Al film only on GaAs. Light emission studies have shown that the emission efficiency depends on the quality of the interface layer. Pulsed-laser experiments for the generation and excitation of electron-hole pairs have demonstrated the importance of charge trapping in an interface region extending more than 100 Å into the oxide.

CHAPTER I

INTRODUCTION

As was outlinded in the previous Final Technical Report[1], efforts of producing stoichiometric interface regions, i.e. a sharp transfer from GaAs to Ga_2O_3 + As_2O_3 or any other insulator without for example elemental As accumulation, led to a first enrichment with Ga of the GaAs surface by an initial anodization and annealing in H_2 atmosphere. This method resulted in a capacitance/voltage behaviour for the MOS structures thus produced which gives even for relatively high frequencies of around 100 Hz capacitance values resembling those of an inversion[2]. Further work in this field has now shown that the same results can occasionally also be obtained by producing an Al_2O_3 film via Al evaporation and anodization without deliberately enhancing the Ga concentration on the GaAs. These results are described by Chapter 2.

Simultaneously it was found that the electroluminescence, reported by us on GaAs MOS and Schottky structures, is an indication of the quality of the transition. These results are given in Chapter 3.

Realizing the importance of obtaining more information on this interface layer, transient studies of MOS diodes with pulsed laser generation or excitation of electrons and holes were undertaken.

This work gave evidence for the electrical activity of a substantial interface film so that a refined model was set up for charging effects affecting capacitance voltage characteristics so that possibly even inversion-type values could be obtained. These details are presented by Chapter 4.

The experimental data now available both by many other authors as well as by us, as described by our previous ERO report and the present one, suggest therefore that it is unlikely that the Fermi level at the interface of GaAs MIS structures can be moved to inversion or accumulation conditions. The promising capacitance/voltage results observed by us and other authors are therefore likely to still be so substantially affected by trapping at this interface layer that it will be difficult to achieve satisfactory microwave inversion type MISFETs. Therefore it is recommended here to undertake in future first a more concentrated effort on microscopic reactions during deposition of films on GaAs using such analytical tools as ESCA. These conclusions and recommendations are given in Chapter 5.

CHAPTER II

The Effect of Fabrication Steps on Capacitance Behaviour of GaAs MOS Diodes

Both n and p type GaAs was employed. First the ohmic contact was deposited after cleaning of the semiconductor surfaces in acetone and dried in a beam of nitrogen. Metals were evaporated in a system using a turbo-molecular pump at about 10^{-6} torr. The metals consisted of 2000 Å Au-Ge (88 %/12 %) for n-type material and 200 Å In + 2000 Å Ag for p-type GaAs.

Subsequently, after a further careful cleaning and treatment of the GaAs surface, an aluminum thin film was evaporated. This film was then oxidized by the so-called AGW-method as described previously[3]. Finally on top of this Al_2O_3 layer, a further thin layer of aluminum was evaporated through a mask resulting in 2000 Å thick and 0.25 mm^2 circular metallic dots to obtain the required MOS structures.

Similarly MIS diodes were also grown with native oxides in order to have a direct comparison for the two types of structures available.

The capacitance voltage relation for these devices thus fabricated were obtained by a measurement system incorporating an Ortec-Brookdeal Ortholoc SC 9505 lock-in analyser together with a

Kipp & Zonen BD 31 x-y-x-t curve tracer. The voltage generator producing a triangular bias voltage ramp was made to give $\pm$ 12.5 V amplitudes with a sweep rate of 0.5 V/sec. The measurement frequencies from a broadband signal generator, type SBF BN 40861 of Rohde & Schwarz, ranged from 10 Hz to 100 kHz.

Figures 1 and 2 show then CV characteristics of MIS structures with native oxides for p and n type GaAs, respectively. For comparison purposes both the capacitance of the insulator alone, C_i and of the depletion capacitance for high frequencies: C'_{min} are introduced into both figures.

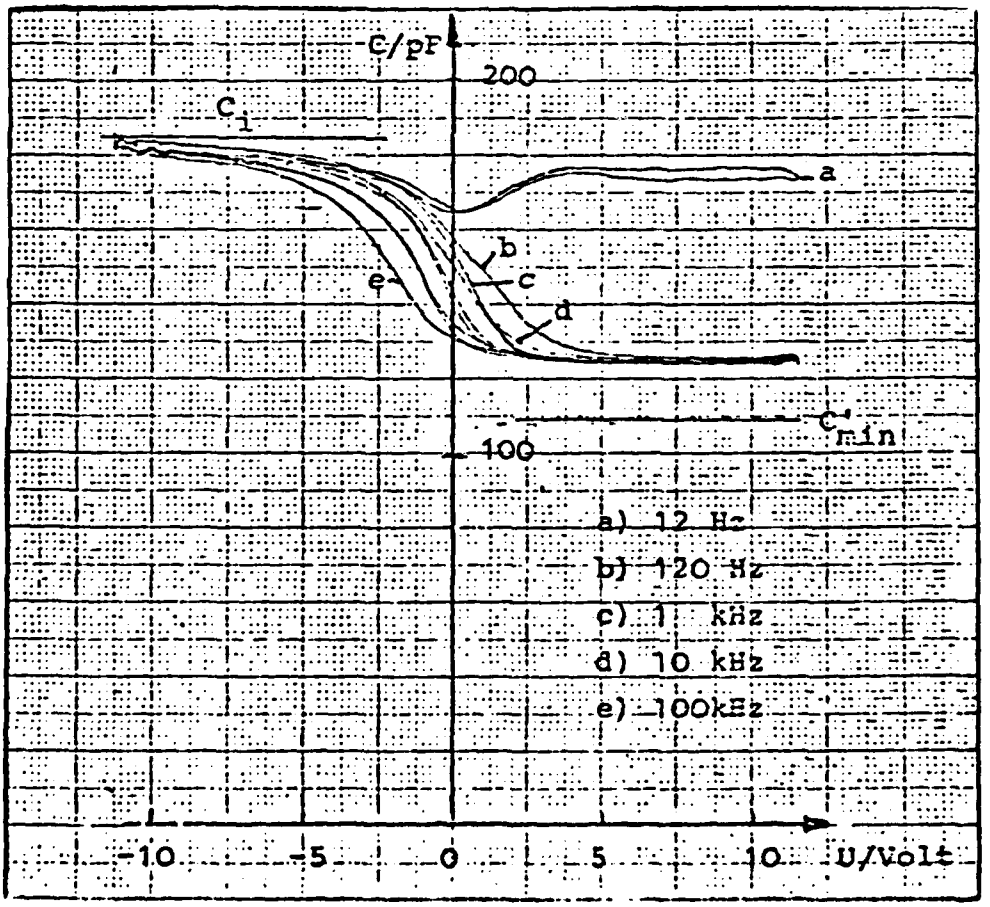


Fig. 1 Capacitance voltage characteristic of MIS structure on p-GaAs, doping density 1.8×10^{17} cm^{-3}

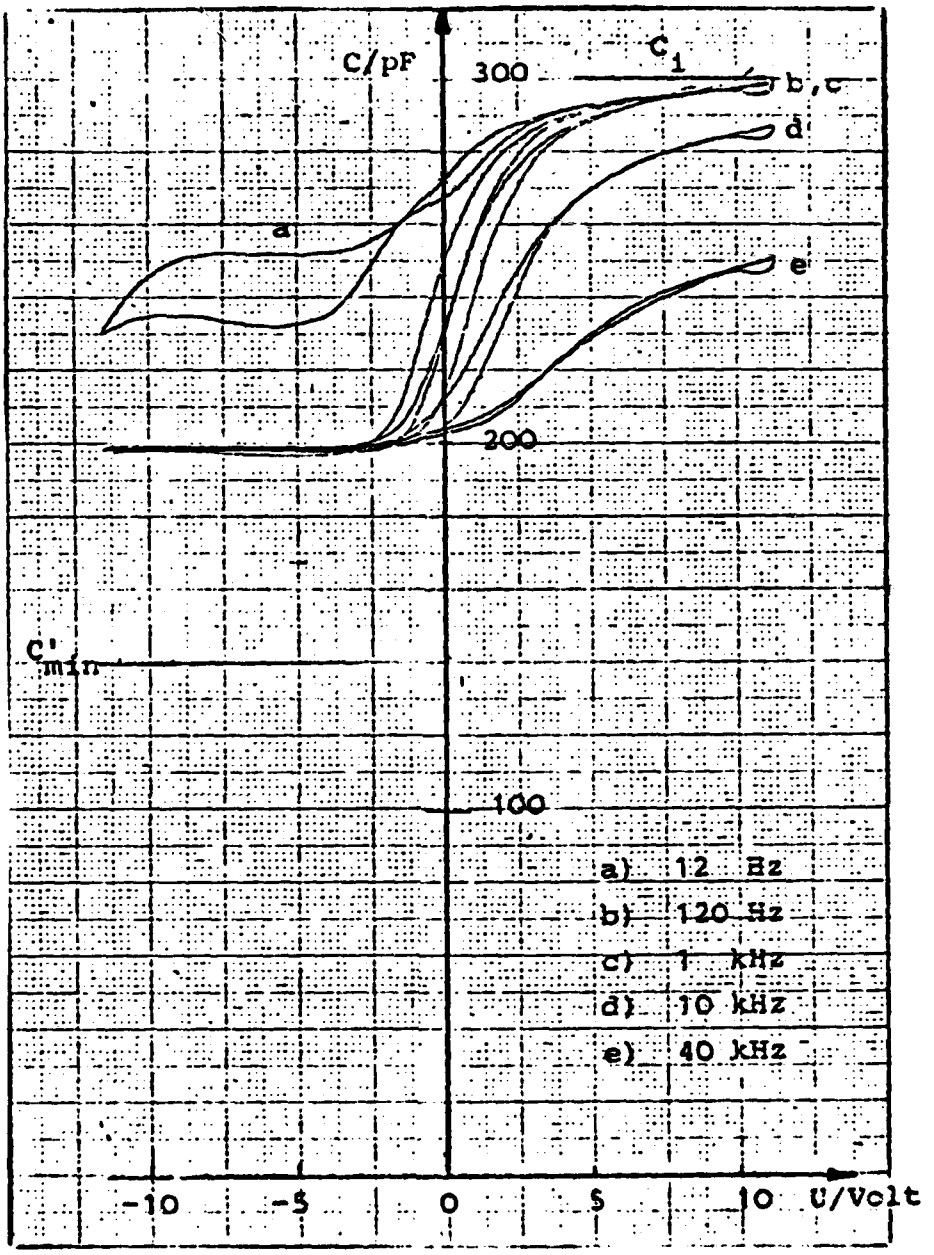


Fig. 2 Capacitance voltage characteristic of MIS structure on n-GaAs doping density 1.7×10^{17} cm^{-3}

These results are comparable to any of the previously published capacitance-voltage characteristics using native GaAs. See for example the data presented in the following references: 4, 5, 6. They are remeasured and reproduced here in order to have a direct comparison available with the MIS structures based on Al_2O_3.

However several points can now be mentioned here by way of interpretation due to the better understanding available than at the time of the writing of the previous references. For the p-type diode of Fig. 1 the measured capacitance of 124 pF for positive bias leads to a differential space charge capacitance of 398 pF since the oxide capacitance is 180 pF. This space charge layer is therefore shorter then could be expected for weak inversion. This could be explained by the concept of Fermi level pinning at the interface, so that the full depletion width cannot be established by applied positive bias. This pinning is caused by both interface states and traps near the interface in both the oxide and the semiconductor (see also Chapter 4). Regarding the n-type sample the analysis of a model based on ref. 7 shows that for n-GaAs MIS structures the accumulation dispersion can also be explained on the basis of such states and traps. In fact a theoretical curve can then be obtained which is very close to the C/V characteristics presented here. For p-type MIS diodes no dispersion is found for accumulation with the frequencies employed. This can possibly be explained by the relatively low time constants of these interface states and traps for p-type MOS structures.

MOS structures based on Al_2O_3 had an insulator thickness of 645 Å based on an Al deposition of 430 Å. The current densities for anodic oxidation ranged from 40 $\mu A/cm^2$ - 120 $\mu A/cm^2$. With the resulting diodes capacitance-voltage characteristics were obtained for different fabrication details. Fig. 3 shows the curves for a diode with the Al_2O_3 layer together with a native oxide at the interface of about 100 Å thickness. Oxidation occured at 60 $\mu A/cm^2$ and subsequent annealing took place in N_2 atmosphere at 375° C for 5 minutes.

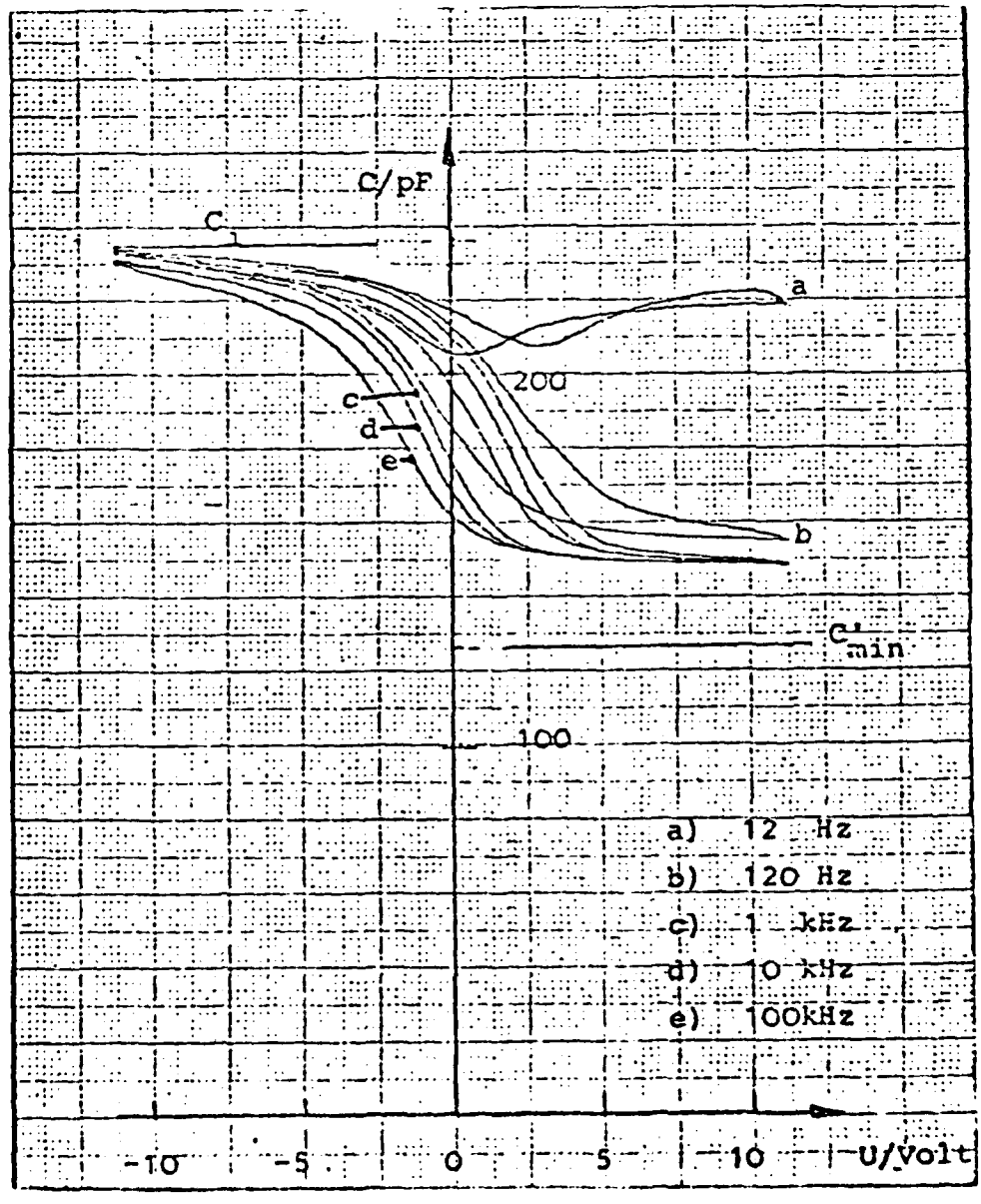


Fig. 3 Capacitance voltage characteristics of Al_2O_3 MOS device with thin native interface layer

Again here the values of C_i and C'_{min} show that Fermi level pinning obviously takes place to a large extent. The relatively large histeresis can be understood on the basis of some charge trapping effect possibly at the interface between Al_2O_3 and native oxide.

Another typical result was obtained by a similar diode as shown by Fig. 4. Here it can be seen that the inversion capacitance is not reached either whereas the accumulation type capacitance is even further removed from the theoretical C_i value. For increasing measurement frequency the depletion type capacitance decreaces continously towards C'_{min} in contrast to the results of Fig. 3, obviously because the time constants for the traps and interface states associated with this sample are ranging into the higher frequency regions.

A third case selected from the many samples tested, is given by Fig. 5 where it can be seen that the frequency dispersion in inversion type and accumulation type bias is relatively small. This can also be explained by very rapid response of interface states and traps so that over all the frequency values of measurement the same result is obtained as established by the previously published model of Fermi-level pinned interface[7].

Further experiments were undertaken with a thin interface layer based on GaN. Here this insulator is produced out of thin native oxide on GaAs in an NH_3 atmosphere at temperatures of 500° C - 600° C. GaN has been produced in the past from Ga_2O_3[8]

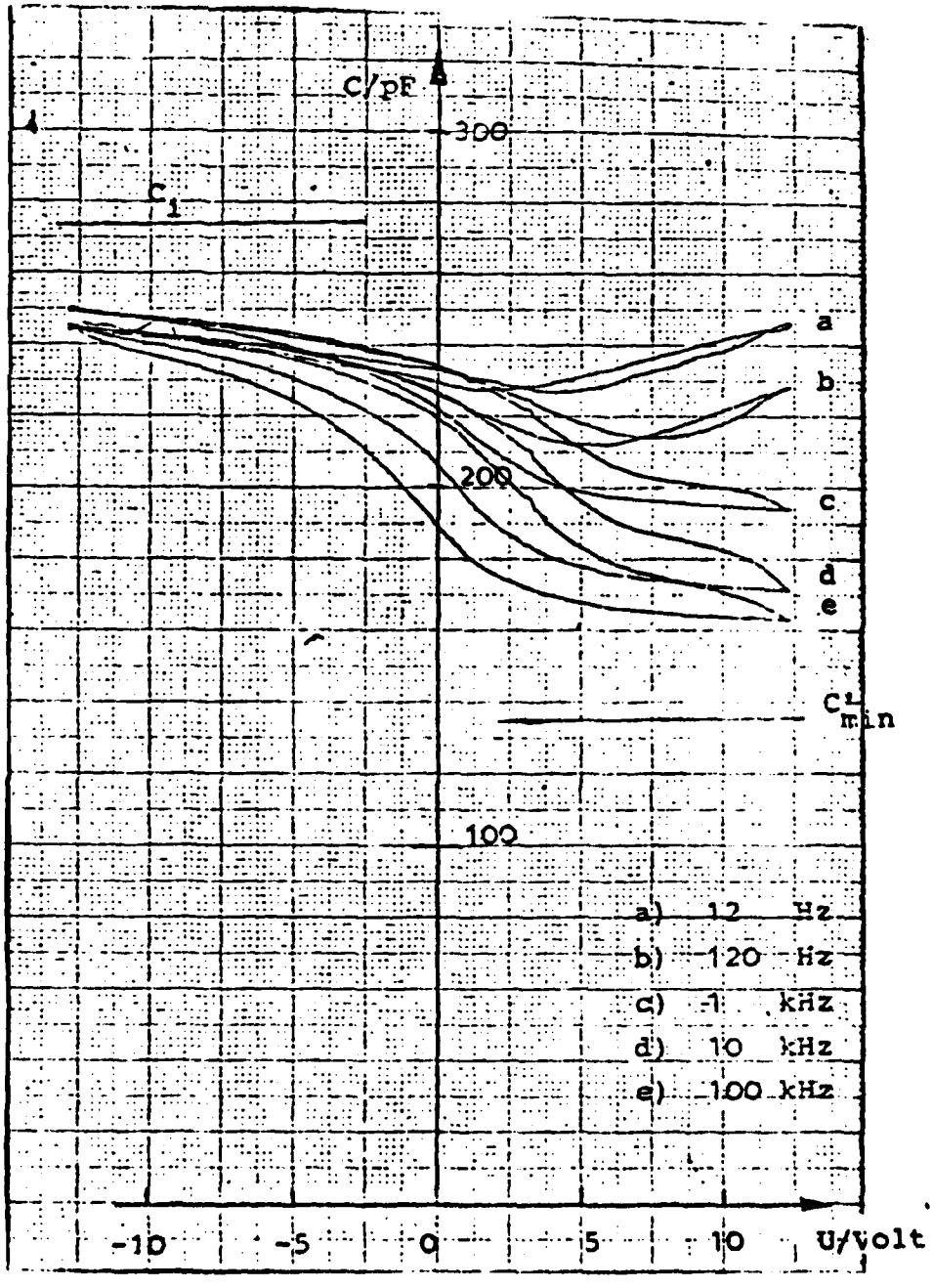


Fig. 4 Capacitance voltage characteristics

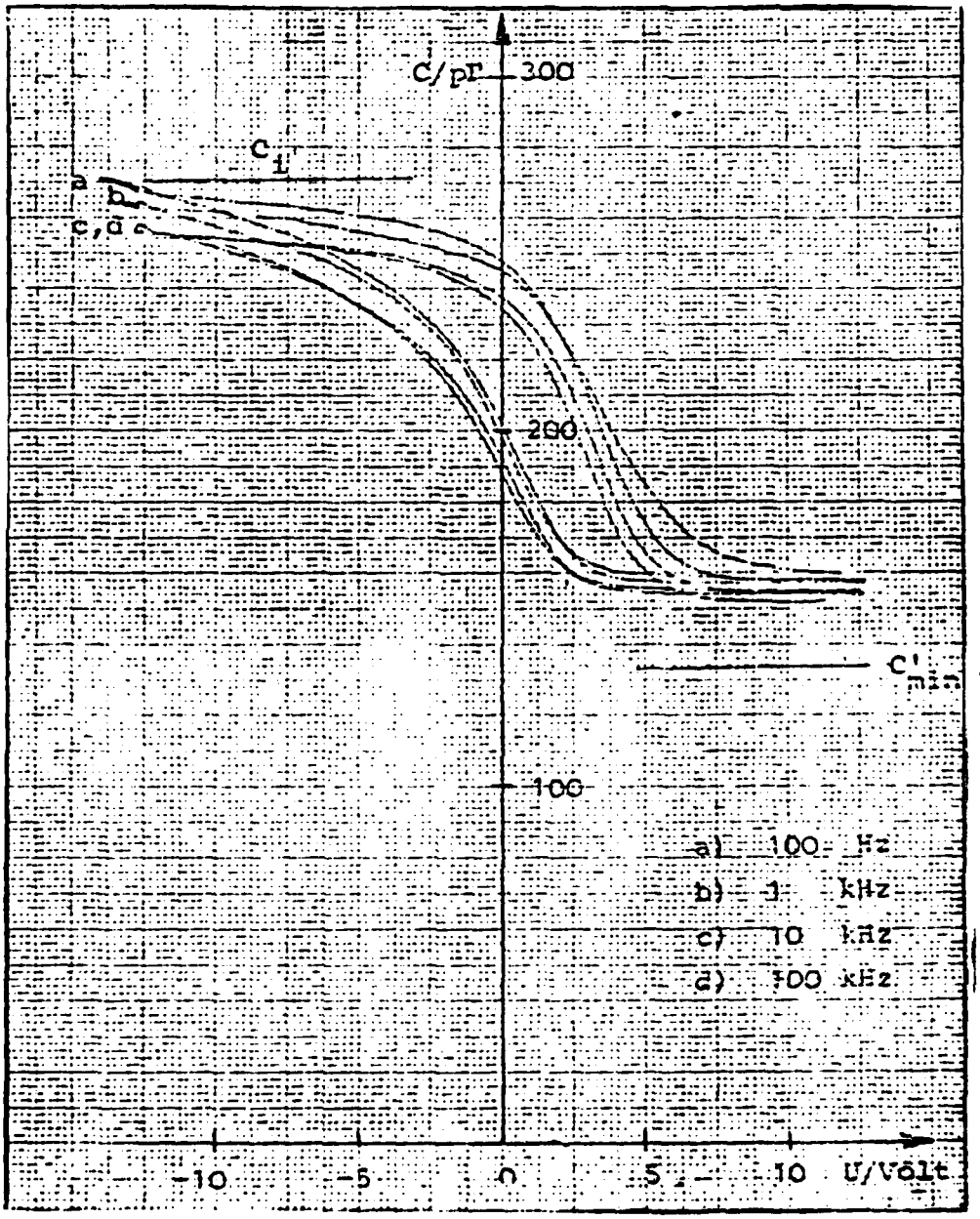


Fig. 5 Capacitance voltage characteristics

according to the following formula

$$Ga_2O_3 + 2\ NH_3 \longrightarrow 2\ GaN + 3\ H_2O$$

Even at temperatures of around 600° C this reaction has a negative equilibrium constant log K(T). This means, that the equilibrium is in favour of the original composition. For the equilibrium constant we have

$$\log K(T) = - \frac{\nu_i G_i^{\circ}}{R.T.\ln 10}$$

according to |9|. Here we have

ν_i	the mol-number of the material participating in the reaction. This is positive for the final material and negative for the initial material
G_i°	molar free enthalpy of the material
R	general gas constant
T	temperature

For the molar free enthalpy we have

$$G_i^{\circ}(T) = H_i^{\circ}(T) - T.S_i^{\circ}(T)$$

where H_i° enthalpy of the material
and S_i° entropy of the material

The values of $G_i^o(T)$ from |9| and |10| are given for two temperatures in Table 1.

	G_i^o (298 K)	G_i^o (800 K)
Ga_2O_3	- 264,8	- 281,5
NH_3	- 24,7	- 50,5
GaN	- 28,3	- 34,8
H_2O	- 71,4	- 96,4

Table 1

Using these values one obtaines for eqn (3)

$$\log K \text{ (298 K)} = - 31,80$$
$$\log K \text{ (800 K)} = - 6,60$$

In spite of the negative equilibrium constant log K substantial amount of GaN was still formed. The reason is probably that H_2O evaporates entirely and the equilibrium is thus moved in the direction of the end products. The production GaN was investigated using Auger-depth-profiling. The results are shown in Fig. 6 and 7.

These MIS structures were used in the following manner after careful cleaning and AGW oxidation giving a native oxide layer of 1000 Å.

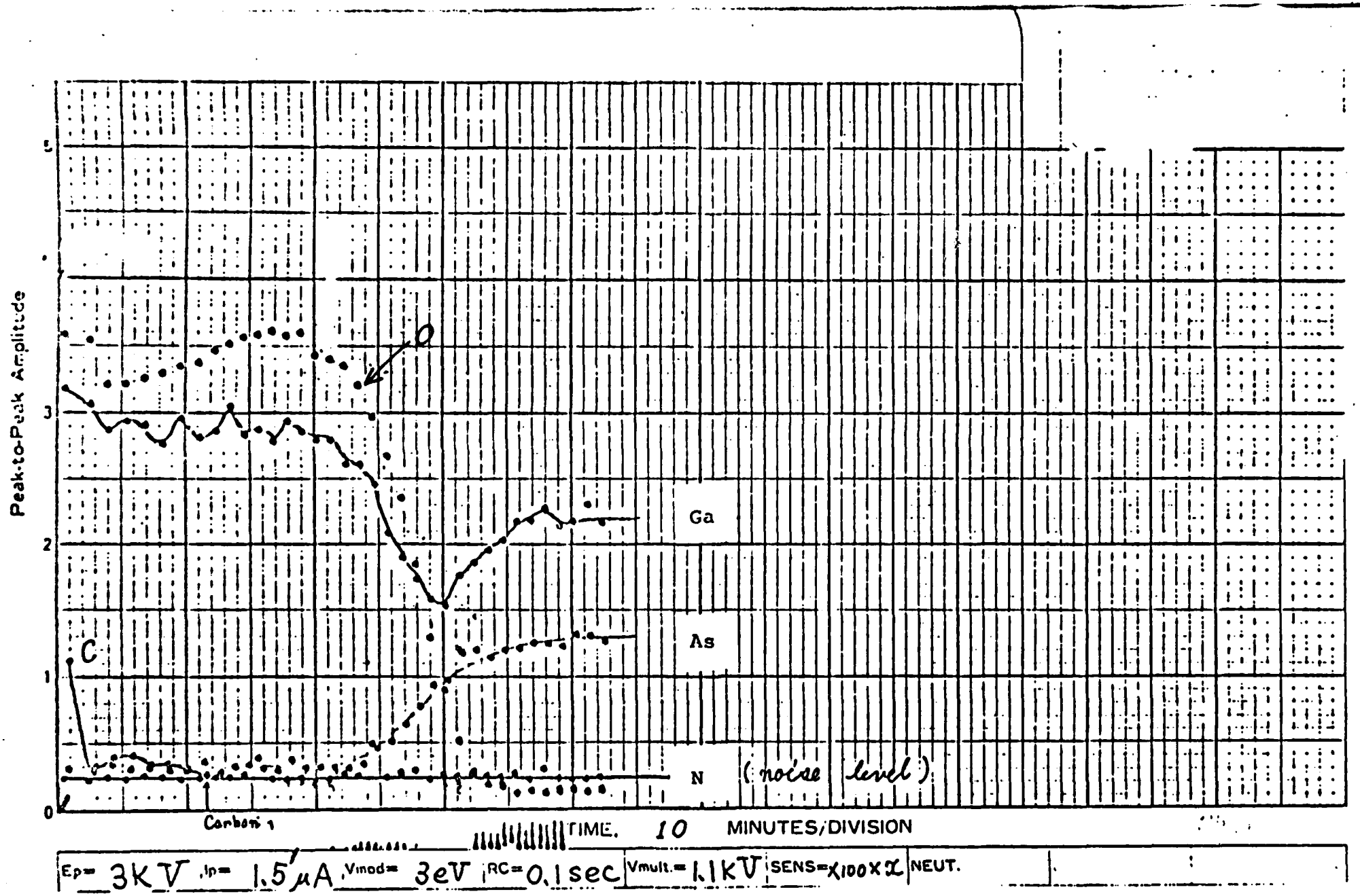


Fig. 6 Auger-Depth-Profile of sample 35S

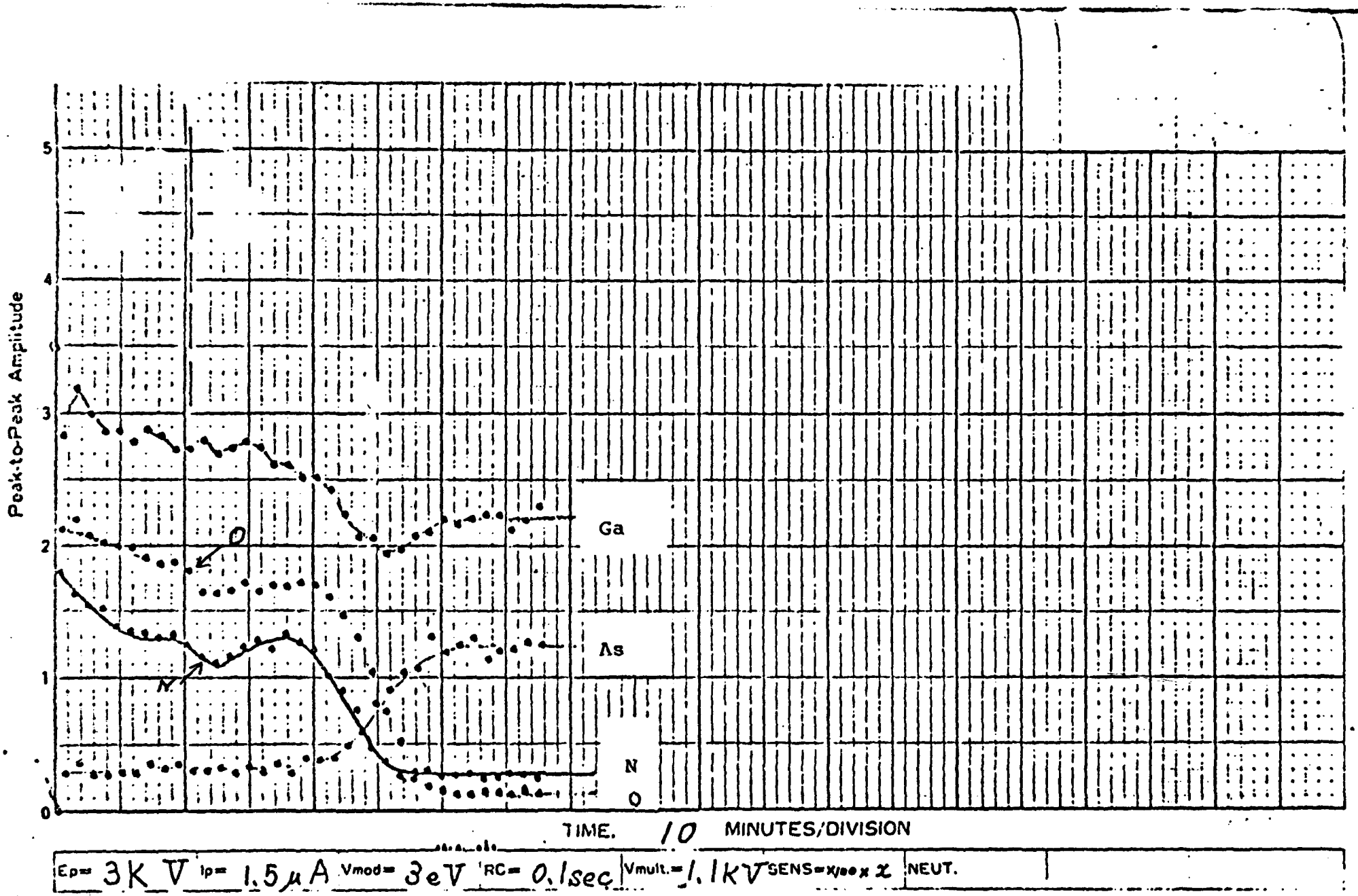


Fig. 7 Auger-Depth-Profile of sample 36S

The samples were heated up to 600° C for the one of Fig. 6 and 650° C for that one of Fig. 7 in an atmosphere of NH_3 at a pressure of 400 torr. Fig. 7 shows that N has reached the interface with the semiconductor. No As atoms were seen anymore in either of the insulator layers. That means obviously all As_2O_3 is evaporated.

Using this technological facility new Al_2O_3 MIS structures were fabricated. Either the originally available native oxide layer of around 10 - 20 Å thickness on GaAs was used to produce GaN films, or a thin native oxid of 50 - 100 Å was first AGW produced. Efforts were also undertaken to initially produce a much thicker native oxide of around 1000 Å so that relatively thick GaN layers were produced as interface. For the oxidation of GaAs the current density of 200 $\mu A/cm^2$ was used.

Fig. 8 shows the capacitance voltage characteristics as produced from the initial native oxide layer on the GaAs sample with an Al_2O_3 layer 645 Å thick. The native oxide layer was transformed into GaN by annealing for 1,5 hours at 500° C. A comparison of Fig. 8 with Fig. 3 shows that no improvement is reached by incorporating a GaN interface layer. Also layers produced by anodic oxidation of GaAs up to a thickness of about 100 Å give similar results as shown by Fig. 9 and 10. Remarkable is here that a relatively large histeresis is found. MOS diodes with an interface layer produced from a 1000 Å native oxide thick film do neither produce any improvements.

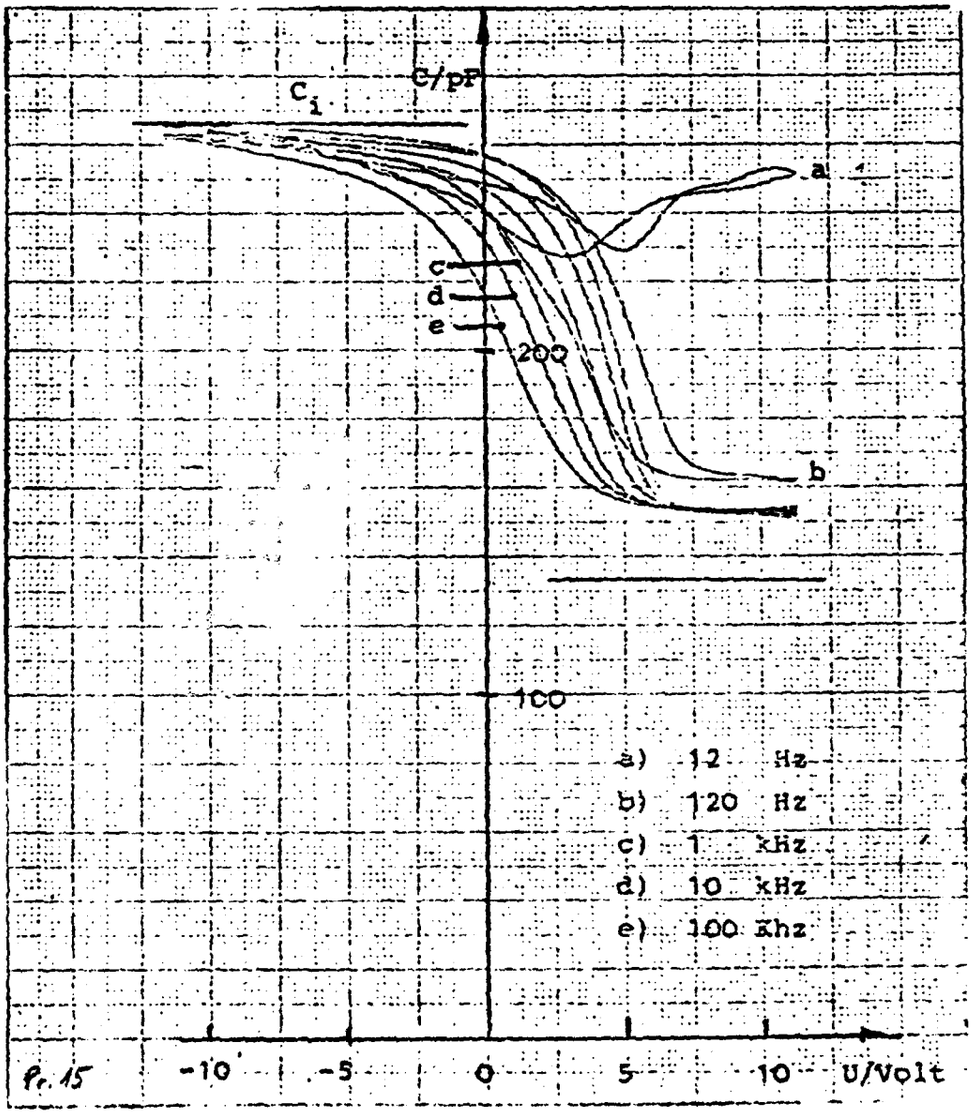


Fig. 8 Capacitance voltage characterisitic of Al_2O_3 MOS structure with GaN interface layer

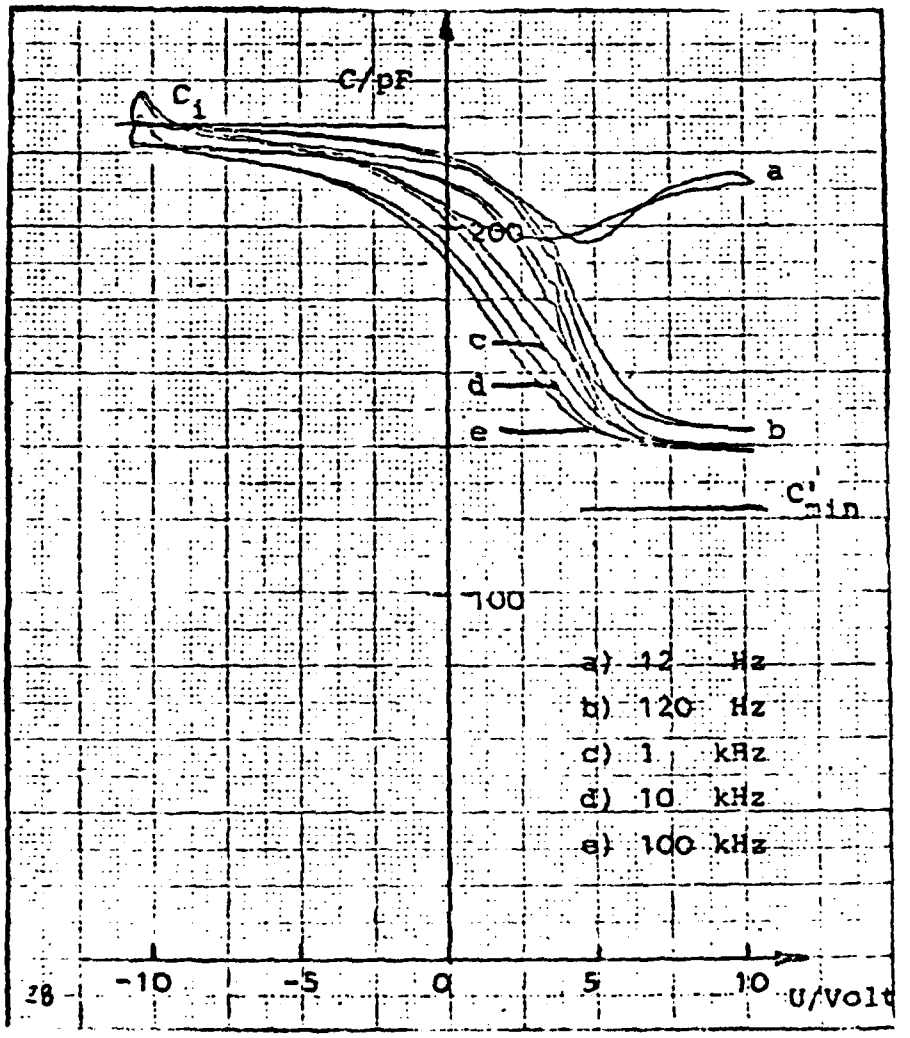


Fig. 9 Capacitance voltage characteristic with a 100 Å thick GaN interface

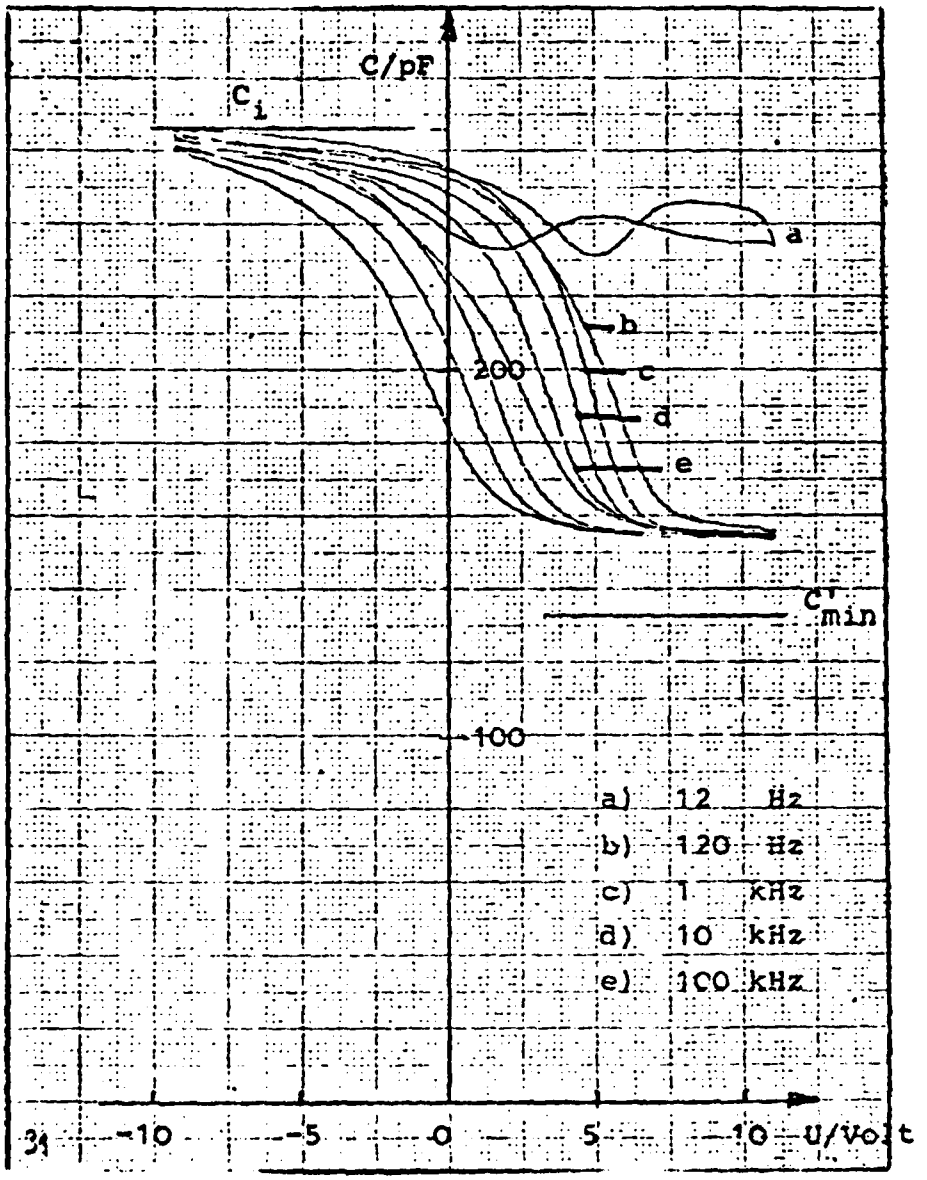


Fig. 10 Capacitance voltage characteristic with a 100 Å thick GaN interface

Only when the annealing time in connection with an NH_3 is increased to 16.5 hours an interesting change in C/V characteristic for such a 1000 Å thick initial native oxide layer results as shown by Fig. 11. Here again the positive bias voltage does not lead to the theoretical inversion capacitance value. However, the capacitance at low frequencies increases more strongly than seen with the previous results. It is possible that this is based on a smaller time constant of interface and trap states; however, it is also feasable to argue that this now shows some inversion type behaviour. The hesteris is relatively small.

The structures as given by Fig. 5 and 6 were now subsequently annealed at 600° C for 2 hours in NH_3. This did produce some demage on the free insulator but the resulting C/V characteristics are shown now on Fig. 12 for the case of Fig. 5. It can be seen that some important changes in the behaviour occured. The accumulation-type capacitance was increased. This might be a reduction of the insulator film thickness or an increase of the dielectric constant of the insulator due to annealing. For positive bias the dispersion characteristics could mean a reduction of interface state or interface trap densities. It could of course also mean a change in the time constant of trap and interface charging and detrapping. The histeresis is considerably reduced.

The results reported here show that the capacitance voltage characteristic can indeed be modified by various treatments of the interface before depositing Al_2O_3. However, this effort has

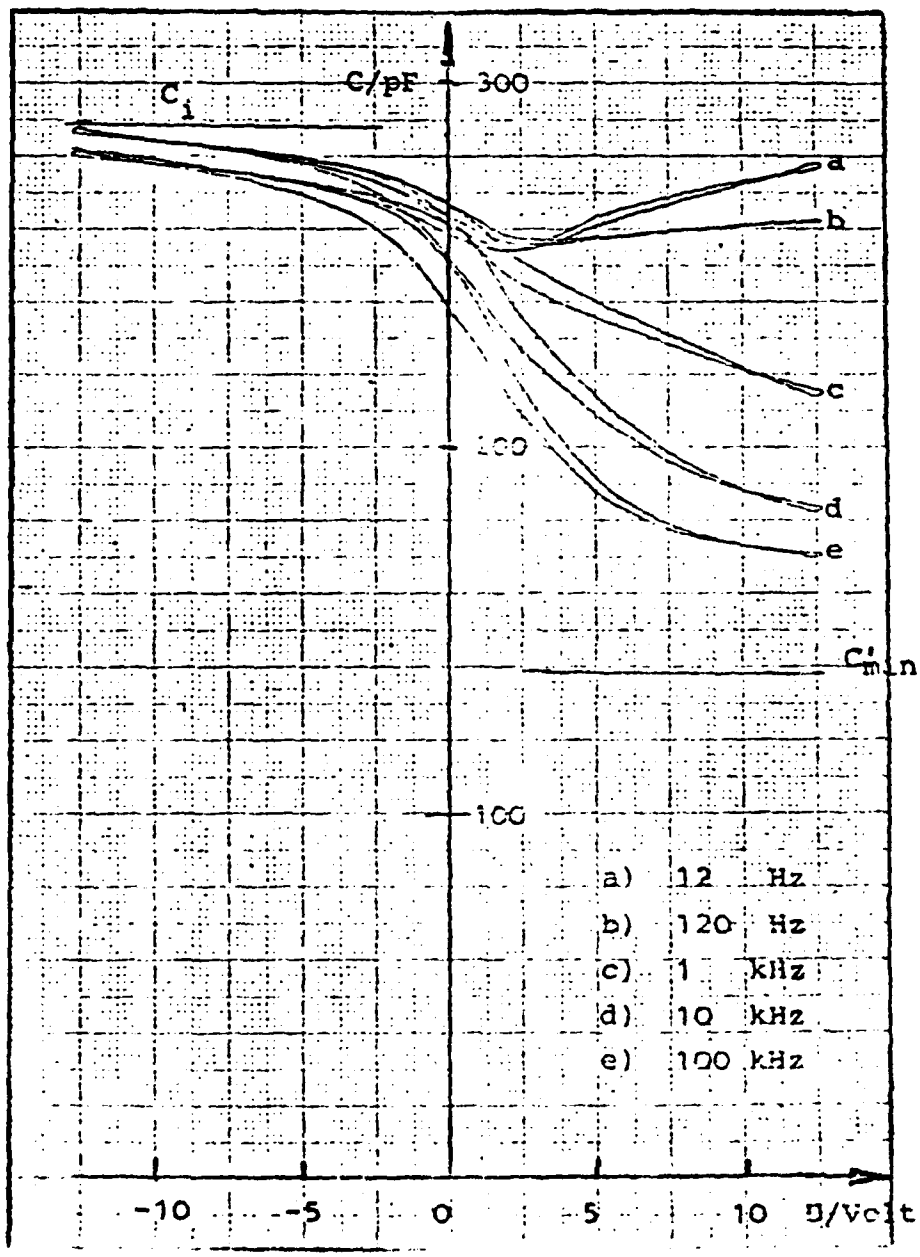


Fig. 11 Capacitance voltage characteristic of thick GaN interface with long annealing time

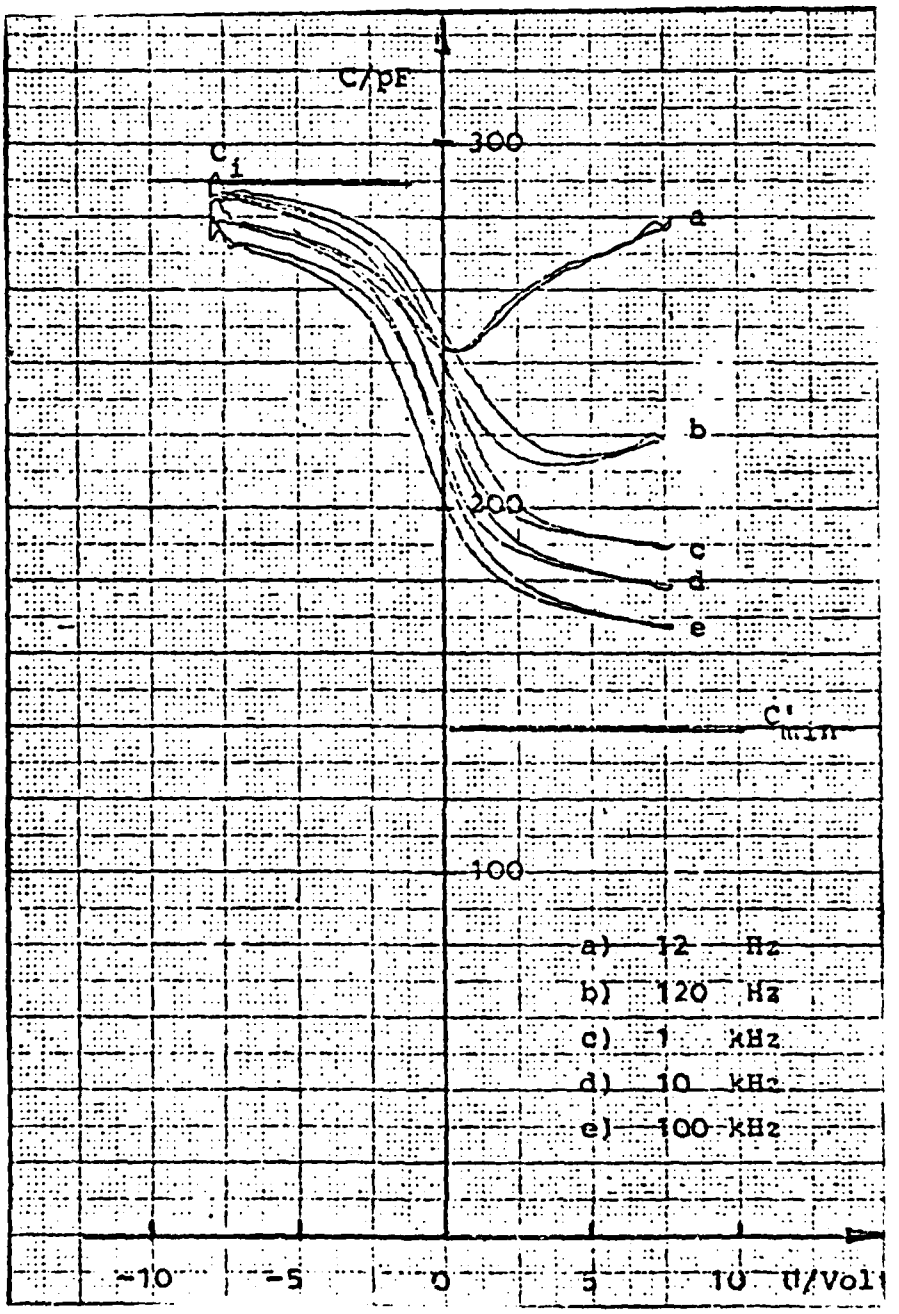

C/pF
300
C_i
200
100
a
b
c
d
e
C'_{min}
a) 12 Hz
b) 120 Hz
c) 1 kHz
d) 10 kHz
e) 100 kHz
-10
-5
0
5
10
U/Volt

Fig. 12

also shown that a truely unambiguous movement of the Fermi level at the interface cannot be achieved since the dispersion observed, the insufficiently small accumulation type capacitance values measured and the very low deep depletion capacitance values not reached can all be interpreted on the basis of the previously published model[7] by strong Fermi level pinning as seen by pure native oxide MOS structures.

A similar investigation using, however, only thin native oxides was undertaken in order to study the current-voltage characteristics for diodes with Al electrodes. The oxide layer had a thickness up to 300 Å both in GaAs with $2.6 \cdot 10^{17}$ cm^3 and p material with $2.3 \cdot 10^{17}$ cm^3 was employed. The oxide was again AGW anodically produced. It was found that oxide layer thicknesses up to 60 Å produced an ideality factor of 1.1 of this thin interface insulator. Electrons can tunnel through the insulator and the voltage drop across it remains small. The ideality factor is primarily determined through the non-ideality of the metal semiconductor transition. For insulator thicknesses ranging from 60 - 80 Å the ideality factor reaches the value of 1.2. Here the influence of the insulator material is strongly noticeable. It is shown that from 0 - 80 Å the states at the interface between semiconductor and oxide are in equilibrium with the metal[11]. Fig. 13 shows that our n factors determined in this thickness range correspond to the theoretical line as predicted by Card and Rhoderick[11].

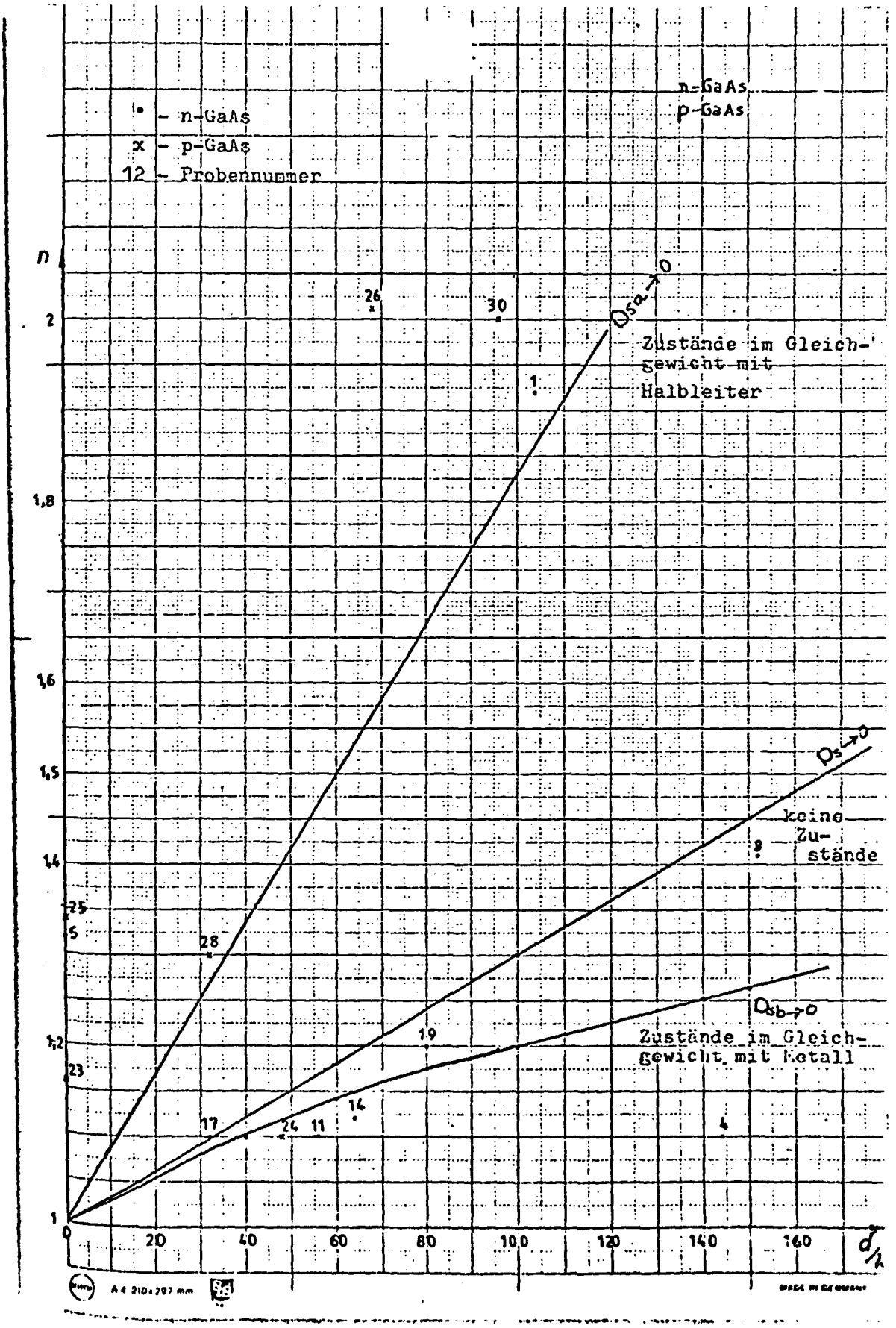

• - n-GaAs
x - p-GaAs
12 - Probennummer
n-GaAs
p-GaAs
n
2
1,8
1,6
1,5
1,4
1,2
1
0
20
40
60
80
100
120
140
160
d/λ
Qsa→0
Zustände im Gleich-
gewicht mit
Halbleiter
Qs→0
keine
Zu-
stände
Qsb→0
Zustände im Gleich-
gewicht mit Metall
26
30
1
28
25
5
19
23
17
24
11
14
4
A4 210 x 297 mm

Fig. 13

For oxide thicknesses between 80 and 150 Å part of the surface states are now only in equilibrium with the semiconductor according to the theory by Card and Rhoderick[11]. This now leads to an increase in the ideality factor to n = 1.4. Finally devices with oxide layers thicker than 200 Å cannot be treated any more unambiguously by an ideality factor since now new processes of current flow associated with Pool Frankle effects and similar phenomena would have to be used in order to understand electron transport across these films.

Also the saturation current, Richardson constants and the barrier-hight are measured. They require an inclusion of the ideality factor for their interpretation. The Richardson constant reduces with increasing oxide thickness.

The saturation current as a function of oxide layer thickness is given by Fig. 14 for the samples prepared.

Efforts were also undertaken to deposit SiO_2 on GaAs by spinning on suitable emulsions and annealing them at various temperatures. Various capacitance-voltage results were observed, some of them with promising inversion-type of characteristics. However, also here the results can be explained by a pinned Fermi level where interface states and traps give a similar behaviour as a mobile Fermi level.

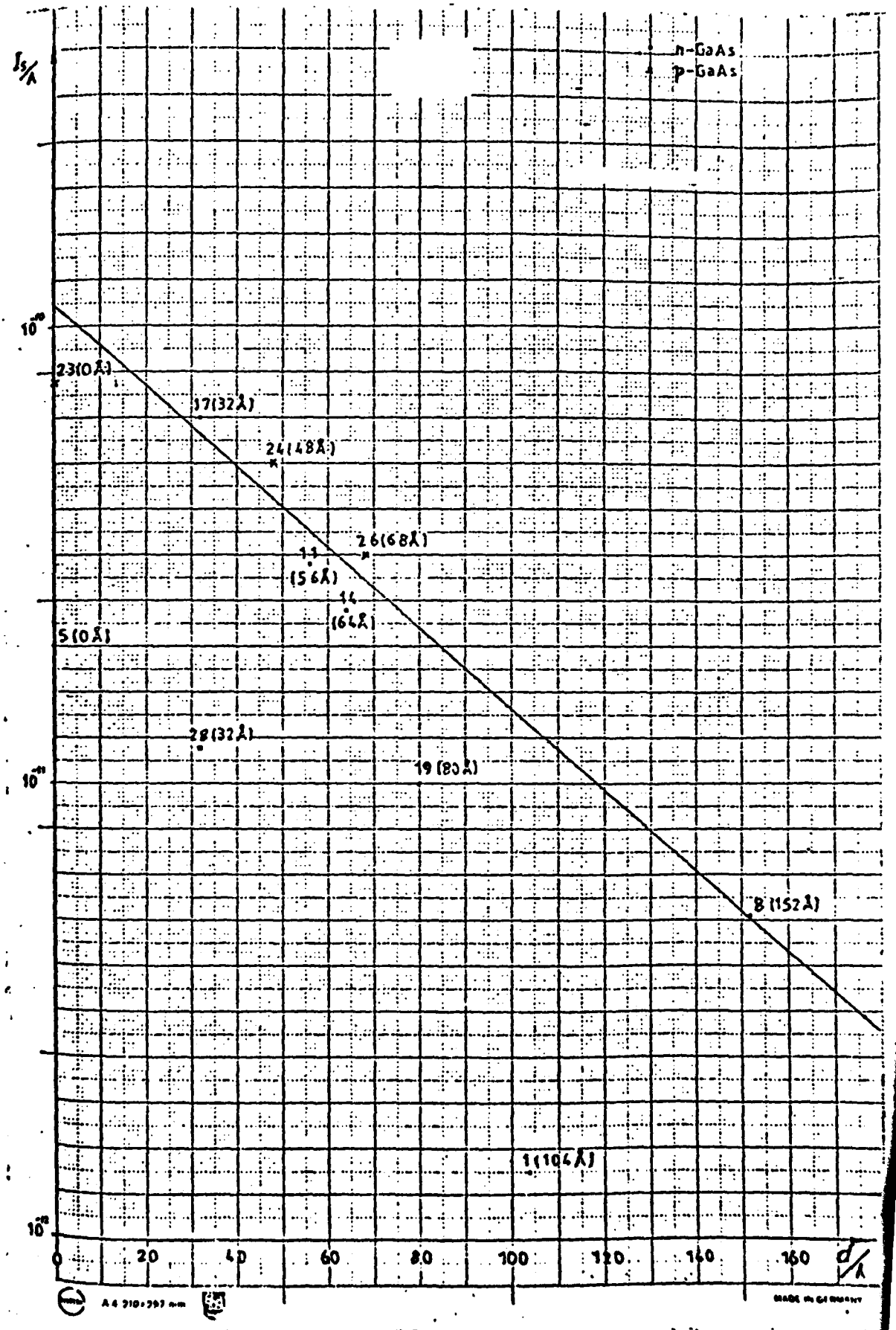

n-GaAs
p-GaAs
I_S/A
10^{-20}
10^{-21}
10^{-22}
23 (10 Å)
17 (32 Å)
24 (48 Å)
26 (68 Å)
11 (56 Å)
14 (64 Å)
5 (0 Å)
28 (32 Å)
19 (80 Å)
8 (152 Å)
1 (104 Å)
0
20
40
60
80
100
120
140
160
d/Å

Fig. 14

CHAPTER III

Electroluminescence from GaAs MOS and Schottky Structures

Further to the results presented in our last Final Report[11] it has now been clarified quite reliably that the light emission originates in the GaAs at the point where electron-hole pairs are created due to avalanching under the very high field at the interface. It is therefore not surprising that we found evidence that the emission efficiency seems to be affected by the quality of the material near the interface.

This work is not only relevant for oxides and other insulators on GaAs but also for metals on compound semiconductors as used for example with MESFET's.

We present initially the essential experimental data, then we adopt the theory of Wolff[12] for our system of light emission and finally we bring additional experimental observations and use them to suggest further efforts on this subject.

Both n and p-type GaAs with carrier densities ranging from 10^{16} cm^{-3} to 10^{18} cm^{-3} was used to fabricate Schottky diodes where the Schottky contacts are circular dots of Al or Au with a thickness of around 2000 Å, produced by evaporation through Mo schadow masks in a vacuum of 10^{-6} torr. On the opposite side of the GaAs slice of typically 0.5 mm thickness a large-surface ohmic contact

of Au-Ge is deposited before the manufacture of the Schottky electrode so that the required annealing temperature does not need to be experienced by the Schottky contact.

The d.c. current-voltage and capacitance-voltage characteristics are then of two types as shown by Fig. 15 for two representative examples (samples 085 and 086). For the types given by sample 085 the capacitance-voltage curve shows a hysteresis, and the current-voltage exhibits a reduced breakdown voltage and a reduced forward current. This type of diode does not give any light emission. On the other hand diodes of the type as given by sample 086 (here 086 is made on the same wafer as 085, but the GaAs is treated differently before evaporation of the Schottky contact as shown below) do not show any capacitance hysteresis, have a higher breakdown voltage and a more ideal forward behavior. The former type (represented by sample 085) does not emit light, whereas the latter one does.

The intensity of the emitted light was measured with a quantum photo meter (Princeton Appl. Res. Model 1140) and a photo-multiplier (Hamamatsu R 928). The current of the photomultiplier is approximately proportional to the intensity of the light. The spectrum of the emitted light was determined by a grating mono-chromator (Oriel, model 7241) together with the quantum photometer. The optical spectral analysis system was calibrated by measuring the light from a tungsten lamp of known spectral emission function.

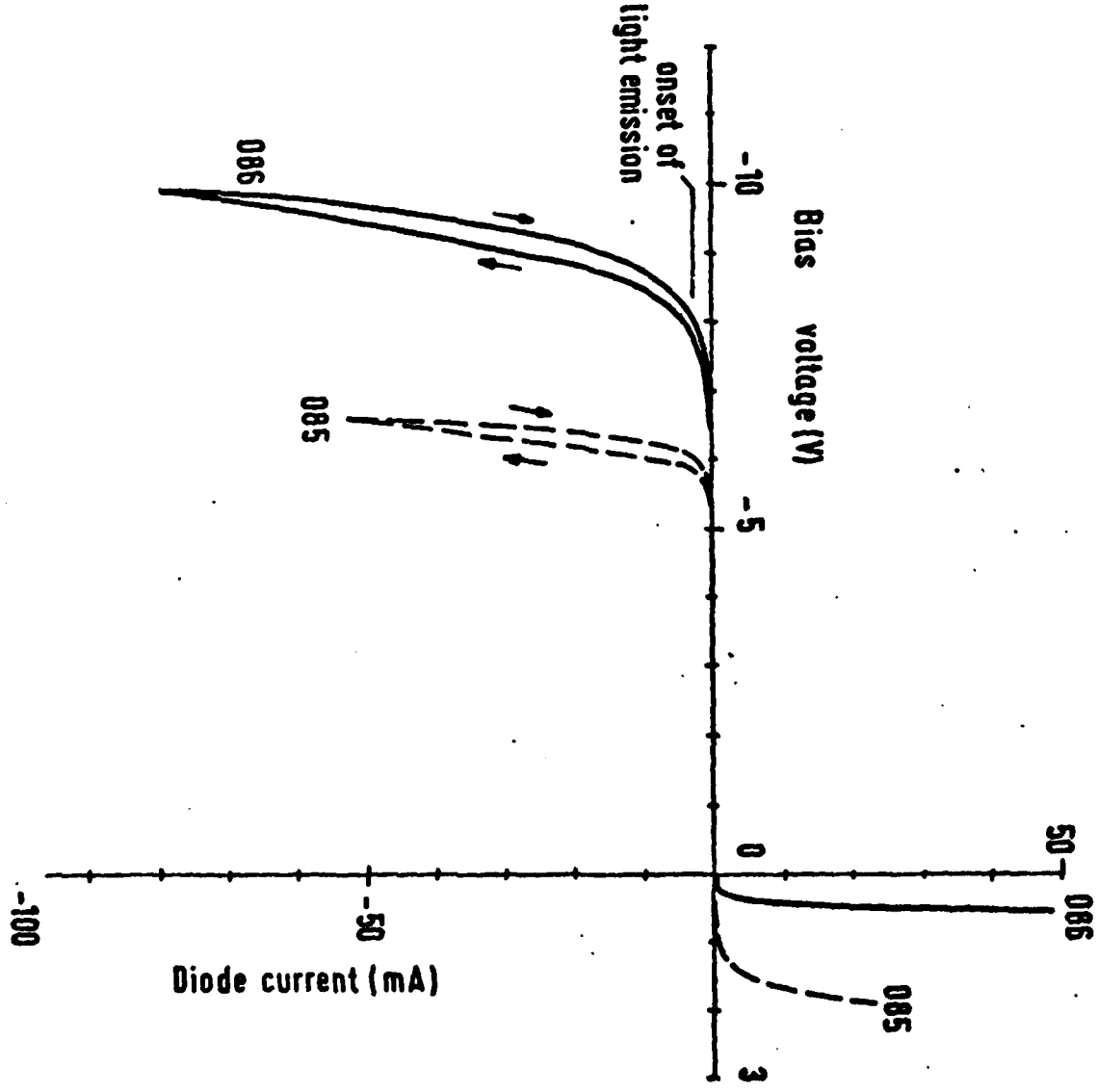
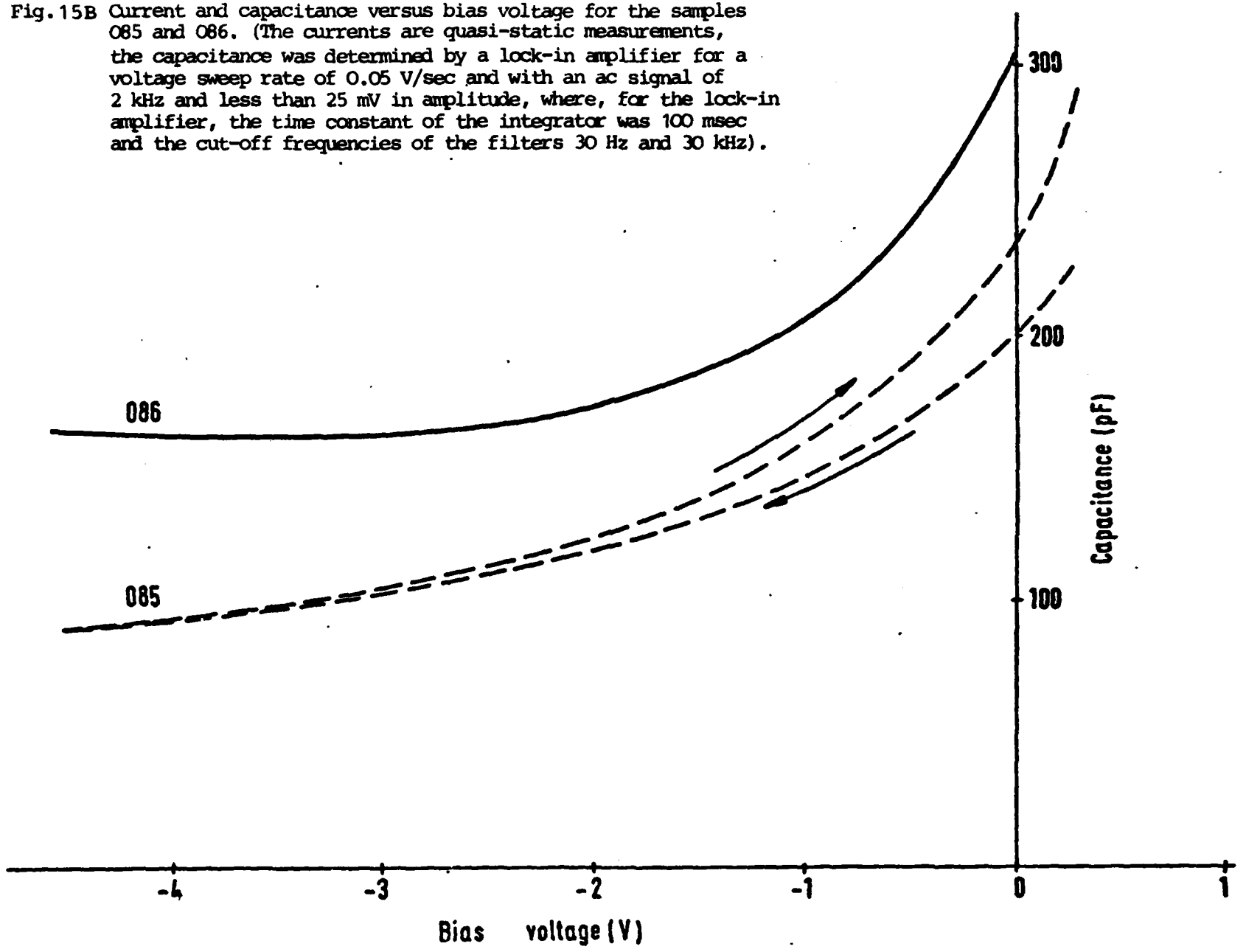


Fig. 15A Current and capacitance versus bias voltage for the samples 085 and 086. (The currents are quasi-static measurements, the capacitance was determined by a lock-in amplifier for a voltage sweep rate of 0.05 V/sec and with an ac signal of 2 kHz and less than 25 mV in amplitude, where, for the lock-in amplifier, the time constant of the integrator was 100 msec and the cut-off frequencies of the filters 30 Hz and 30 kHz).

Fig. 15B Current and capacitance versus bias voltage for the samples 085 and 086. (The currents are quasi-static measurements, the capacitance was determined by a lock-in amplifier for a voltage sweep rate of 0.05 V/sec and with an ac signal of 2 kHz and less than 25 mV in amplitude, where, for the lock-in amplifier, the time constant of the integrator was 100 msec and the cut-off frequencies of the filters 30 Hz and 30 kHz).



Light emission was only observed for carrier densities of 10^{16} to 10^{17} cm^{-3}, both n and p-type. The light-emitting Schottky diodes gave light after the reverse bias had been increased into the avalanching regime (see Fig. 15). The light intensity is then of course current controlled. The total light intensity as recorded by photomultiplier for several of the emitting diodes (which can be considered typical of the large numbers investigated), is shown by Fig. 16 with the diode parameters given by Table 2. It can be seen that the total emission intensity is almost proportional to the diode current, except for diodes with small emission rates when first some initial, non-emitting current seems to be required to fill some non-radiating traps, before a proportionality is again reached for higher current values.

As can be seen from Table 2 and Fig. 16 those samples exhibit a high emission rate where the GaAs surface was etched by a basic solution before evaporation of the Schottky metal. On the other hand a very low emission rate, if not a total absence of emission, was found for samples with acidically etched GaAs surfaces. This behaviour was consistently found with all the samples investigated of which only a small selection is presented here by Fig. 16. It was also consistently found that samples without emission show a C-V hysteresis, and an I-V behaviour typical of that of Fig. 15 a for 085.

In fact the emission rate is smaller the higher the concentration of the acidic component of the etching solution used. Here

Sample	Chemical used for GaAs surface	Wafer (Carrier density)	Emission intensity	Remarks
009	NH_4OH	$n = 1.7 \times 10^{17}$	strong	
066	AGW (Anodic oxide ≈ 80 Å)	$n = 1.7 \times 10^{16}$	very weak	Heat treated
067	$HCl : H_2O = 1 : 1$	$n = 1.7 \times 10^{16}$	weak	unstable
068	$HCl : H_2O = 1 : 1$	$n = 1.7 \times 10^{16}$	weak	Heat treated
072	$HCl : H_2O = 1 : 1$	$n = 1.7 \times 10^{16}$	absent	
075	AGW (Anodic oxide ≈ 40 Å)	$n = 1.7 \times 10^{17}$	strong	Heat treated
076	$NaOH : H_2O_2 : H_2O = 1:20:50$	$n = 1.7 \times 10^{17}$	very strong	
085	$HCl : H_2O = 1 : 1$	$n = 1.7 \times 10^{17}$	absent	
086	$NH_4OH : H_2O = 1 : 1$	$n = 1.7 \times 10^{17}$	strong	
099	$H_2SO_4 : H_2O_2 : H_2O = 20 : 1 : 1$	$n = 1.7 \times 10^{17}$	absent	
102	$H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 250$	$n = 3 \times 10^{16}$	strong	
103	$NaOH : H_2O = 1 : 2$	$n = 3 \times 10^{16}$	strong	
106	$NaOH : H_2O_2 : H_2O = 1 : 3 : 30$	$n = 3 \times 10^{16}$	strong	
107	$NaOH : H_2O_2 : H_2O = 1 : 3 : 150$	$n = 3 \times 10^{16}$	strong	
117	$H_3PO_4 : H_2O = 10 : 1$	$n = 3 \times 10^{16}$	absent	
118	$H_3PO_4 : H_2O_2 : H_2O = 10 : 1 : 1$	$n = 3 \times 10^{16}$	weak	
124	$NaOH : H_2O_2 : H_2O = 1 : 2 : 50$	$p = 1.2 \times 10^{16}$	weak	

Table 2 A selection of the samples studied as reported in this Chapter

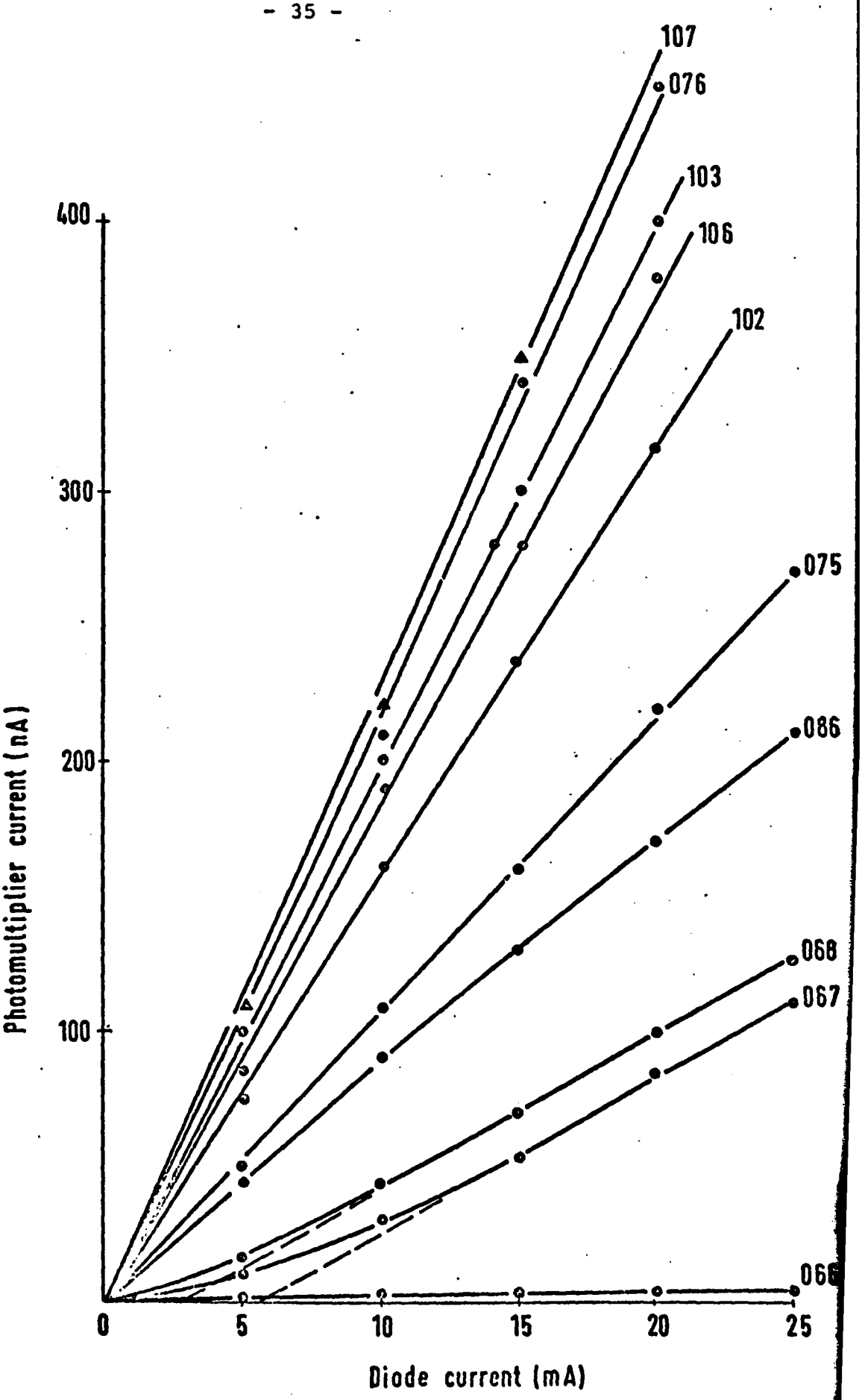


Fig. 16 Total light emission versus diode current for a representative selection of samples whose parameters are given on Table 2

both H_2SO_4 and H_3PO_4 were employed. On the other hand, the inclusion of H_2O_2 in the etch solution increases the emission rate again. Similarly heat treatment of the Schottky contacts in N_2 at 350° C for 5 min. enhances the efficiency. These observations seems to show that the emission rate might be an indication of the composition of the GaAs surface. It is generally known [13] that Ga is not soluble in alkali solution, but soluble in acids. It is, therefore possible that acidic etchants remove more Ga from the GaAs surface than some basic solutions. Similarly, As is solutble in HNO_3 and some other acids whereas it is not clear to the authors what effect basic solutions exhibit on As in GaAs. On the other hand the oxides of Ga are generally more strongly soluble in alkalis than in acids, and oxides of As dissolve in water, thus forming arsenic and arsenious acids. Ga $(OH)_3$ dissolves in diluted acids and has then some basic characteristic. Therefore a native oxide of GaAs seems to loose more Ga in basic than in acidic etchants. One might even suggest that a large and rapid dissolution of arsenic oxide could reduce again the Ga_2O_3 dissolution since As-based acids are then formed. Ga $(OH)_3$ can be expected to occur with wet anodic oxidation, and if its rapid dissolution causes locally basic conditions, the dissolution of Ga_2O_3 is enhanced and of Ga from GaAs is reduced. A more systematic exploration of these details might be valuable in understanding the complex compositional results of various GaAs etch processes.

These superficial generalizations, however, tend to suggest that the high light emission rates for GaAs treated by basic solutions occur since only a reduced interface layer with poor

stoichiometry of GaAs and with native oxide seems to exist then (oxide alone, however, does not prevent light emission, as shown previously[14]). Some confirmation of this hypothesis can be found from the report by C. Chang et al[15].

Wolff[12] showed that the light emission from reverse biased avalanching p-n junctions in Ge is caused by both hot electrons recombining with heavy holes and by hot light holes relaxing into states of heavy holes. These excess carriers are produced by avalanching caused by firstly hot electrons and secondly hot holes after they reached a threshold energy. Since the avalanching process occurs with high probability as soon as an electron or hole has reached its appropriate avalanche threshold, approximately no carriers are found above these threshold energies. This also means that no photons are produced above these energy values. Correspondingly, Wolff established two values of maximum photon energies and he could show that the observed emission spectrum from Ge shows a first onset of photons from the energy for hot-electron avalanching downwards and, superimposed at lower energies, a second onset of additional photons from the energy for hot-light-hole avalanching downwards.

Our emission spectrum shows a very similar behaviour (Fig. 17). At about 315 nm, the photon wave lengths begin, and at about 700 nm a further increase in photon counts occurs. The first threshold is given by the maximum electron energies in the conduction band due to the occurrance of avalanching above the energy E_o. Assuming

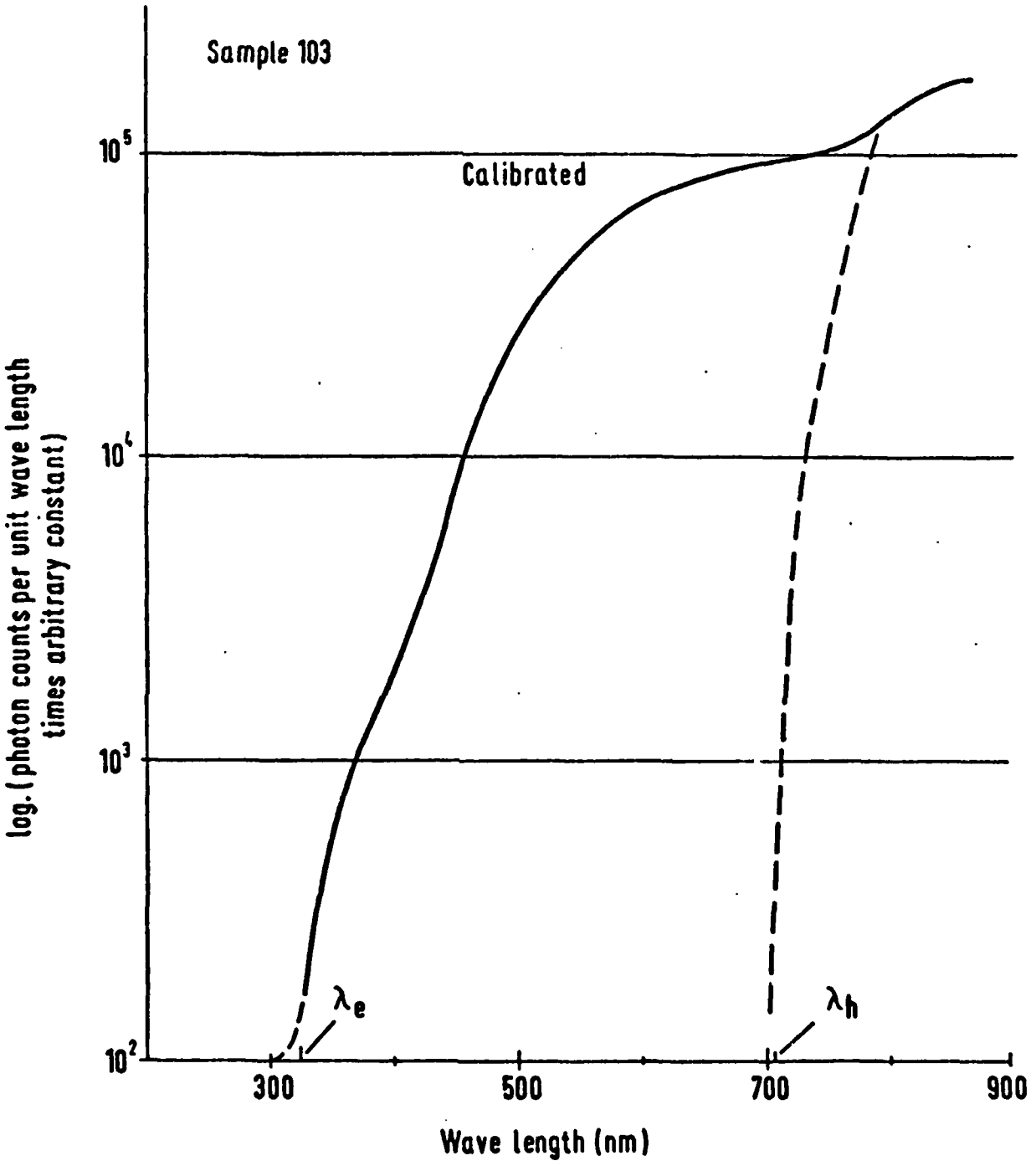


Fig. 17 Emission Spectrum, together with the two treshold wavelengths λ_e and λ_h

a parabolic energy contour as a first approximation for both the conduction band electrons and the valence-band heavy holes, this maximum photon energy is

$$\omega^{e}_{max} = E_o \left(1 + \frac{m_c^*}{m_2^*}\right) + E_G$$

where m_c^* and m_2^* are the effective electron and heavy-hole masses respectively and E_G is the energy gap.

Using the computed values of E_o by Anderson and Crowell[16] for the appropriate orientation (100), and the appropriate parameters for GaAs[17], we find for ω^{e}_{max} a wavelength λ_e - 320 nm. Similarly, for the transition from light-hole states to those of heavy holes, we obtain a threshold energy

$$\omega^{h}_{max} = E_o \left(1 - \frac{m_1^*}{m_2^*}\right)$$

where m_1^* is the effective mass of light holes.

This yields a threshold wavelength λ_h of 720 nm. Both values are in resonable agreement with the experimental finding for practically all the samples investigated (see Fig. 17 for sample 103). This agreement suggests that Wolff's model for the light emission is also applicable here.

The interpretation advanced here for the observed light emission suggests to search for further experimental properties. The points advanced here are suggestions for further work, together with some further details of observed data.

Firstly, it can be expected that some changes in λ_e and λ_h occurs due to a difference in orientation of the GaAs surface, since E_o can be expected to alter then. A change in the spectral distribution function can be expected by altering the GaAs-surface properties. If for example, many non-radiative recombination processes compete with the electroluminescence, this would have a particularly strong effect in cold electron-hole recombinations. It can also be expected that for relatively short space charge-layers in the GaAs, that the charge-carrier transport processes will be affected by short-distance effects. This will result in a modification of the population distribution and correspondingly in a modification in the emission spectrum without primarily affecting λ_e or λ_h. On the other hand, short-distance effects could affect directly the avalanching and electroluminescence processes so that the spectrum can again be expected to be changed.

Among the many spectra taken, changes can be observed when the photon counts are normalized by the value at the peak of the uncalibrated "raw" function. Some first effort here is reported by Fig. 18.

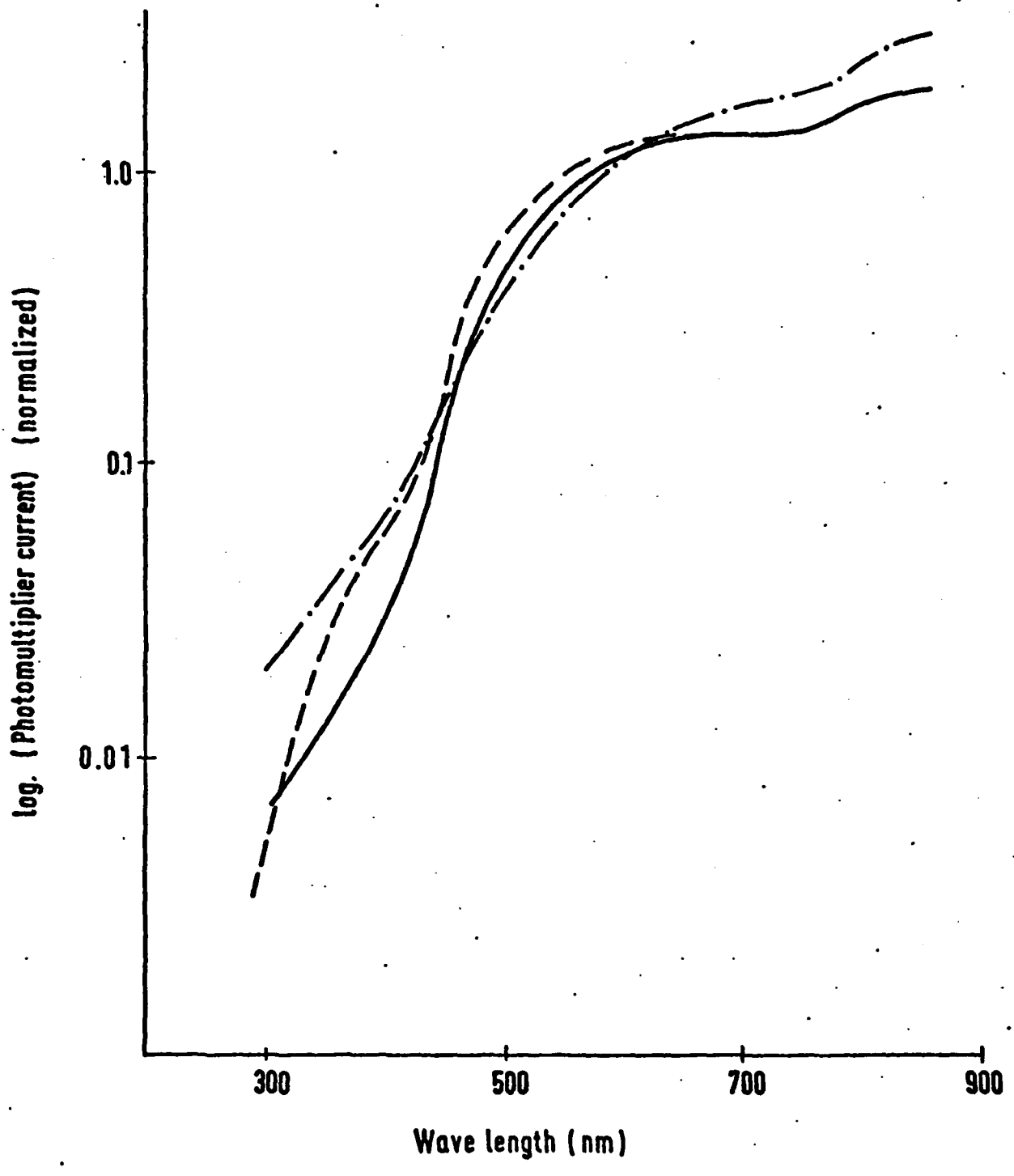


Fig. 18 Normalized spectra for a selection of samples as given in Table 2. (The spectra are normalized by the photon counts at the highest measurement sensitivity from the "raw" curves)

-·-·-·- $n = 1.7 \times 10^{17}$ (sample 009)

——— $n = 3 \times 10^{16}$ (sample 903)

-.-.-. $p = 1.2 \times 10^{16}$ (sample 124)

CHAPTER IV

Pulsed-Laser Illumination of GaAs MOS Structures to Study Charge Trapping

Pulsed laser studies of MOS trapping was undertaken by us incorporating several new features which were not yet part of the work reported so far. For the process of carrier injection into the oxide, the spatial and energy distribution of traps is not known. There are some reports on oxide charging and discharging involving some plausible arguments but so far there is no fully established model to explain the whole phenomenon. The details of charges within SiO_2 over silicon were clarified some time back by extensive studies but insufficient information is only available at present about the charging and discharging properties of traps within the oxide and at the interface of GaAs MOS structures.

We therefore describe here photopulse-response results of GaAs-anodic oxide structures under nonequilibrium conditions. The measurement technique followed is the same as that of Schuermeyer and Hartnagel[17] where they showed that the photo-pulse method can yield the insulator capacitance, some still insufficiently defined interface potential and the semiconductor surface doping density, whereas it is difficult to obtain the insulator capacitance by other methods. However, in our experiment a monochromatic source of light has been used to also investigate the electronic process across the interface. Using photons of a single, well defined energy value, it is possible to gain a somewhat clearer insight into the physical mechanism involved at the interface. A limited range of charging pulse frequency (12 - 120 Hz) of the MIS structure has been studied and the photo-transient response has been analysed qualitatively to explain the observed behaviour of charging and discharging of the semiconductor space charge, the interface state traps and the oxide traps. An energy band diagram is proposed to explain the basic principle of the physics of charging involved here. Throughout this paper only n-type GaAs is used.

The energy-band diagrams, proposed here of a GaAs oxide interface at accumulation- and at depletion-types conditions are shown schematically in Figure 19 where the band-bending is, for clarity of the argument, not to scale. During accumulation-type bias, band-bending is still directed upwards because of pinning of the Fermi level at the interface which is a consequence of the large number of interface states. In addition to these states, there exist traps within the oxide probably due to tne non-stoichiometric formation of the anodic oxide near the interface. The presence of such traps usually seems to be common to all types of oxides and during accumulation bias injection of majority carriers takes place into the oxide where they are trapped at any conveniently situated trap level. As a result the oxide field is distorted, as shown by the dotted line. Even when a short bias pulse is applied, the formation of such an oxide field distribution can occur very rapidly, because of a low equivalent resistance of the charging path and usually also because of tunneling into the defect level in the oxide. There may be traps in the GaAs near the interface as measured by DLTS method by Kamieniecki et al.[18]. This effect has not been included here, but does not basically modify the model presented. The energy band data is based on various recently published experimental data (Aspnes et al.[19] and Yokoyma et al.[20]).

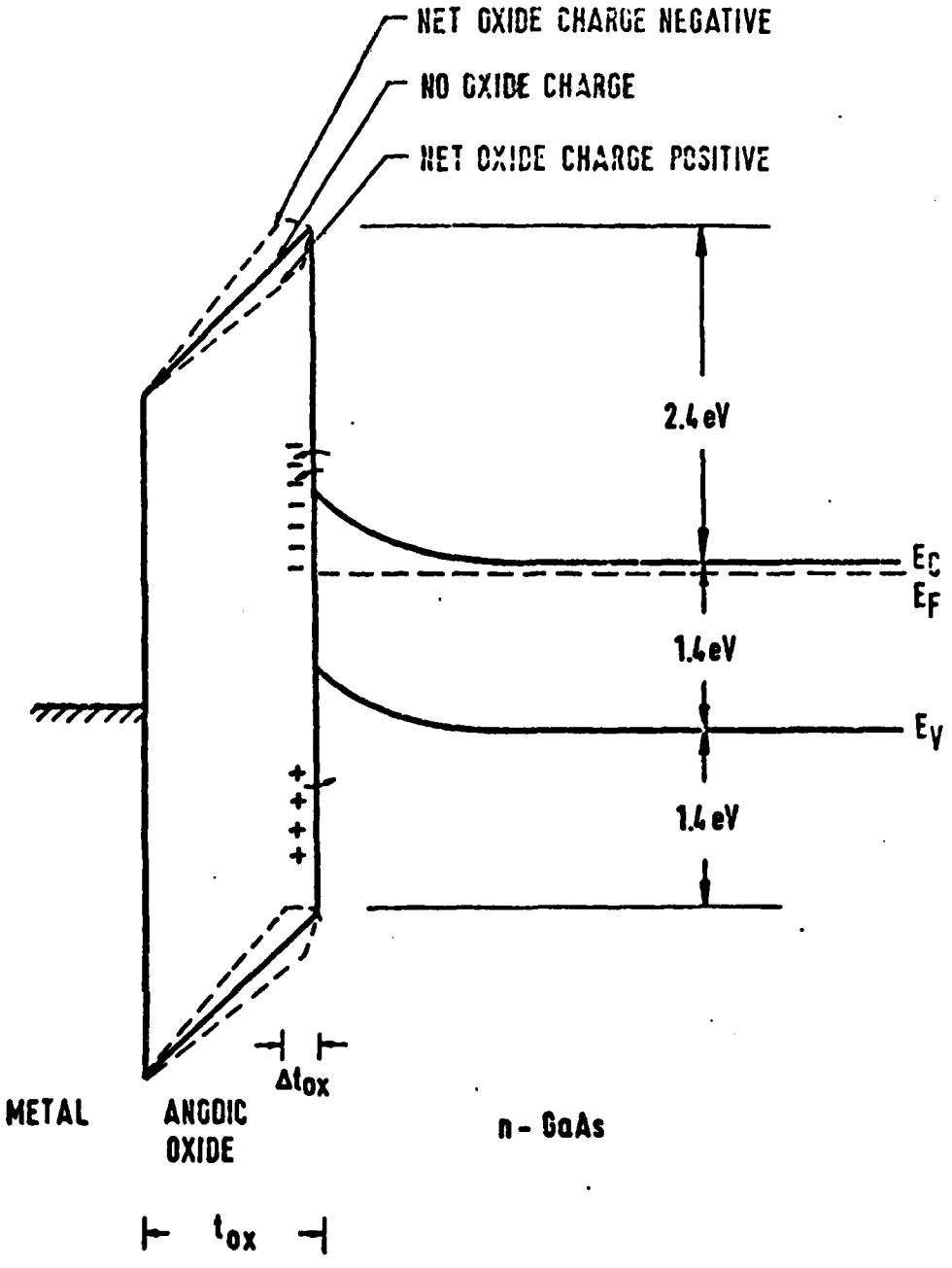


Fig. 19a Energyband diagram of n-type GaAs-anodic oxide-metal structure for pulsed bias and pulsed illumination by a Laser (λ = 632.8 nm) during accumulation-type bias

In Fig. 19b the depletion condition is illustrated for the nonequilibrium condition. The bias is assumed to be changed from accumulation to depletion. Since the potential distribution across the oxide cannot change very fast as this has already been charged, a considerable part of the applied voltage pulse amplitude appears across the semicondutor and a larger space charge layer is formed than for depletion bias at equilibrium. As the oxide charges (majority carriers) are discharged (which happens comparatively slowly), the voltage across the insulating layer changes, as shown there by arrows. Semiconductor band-bending decreases tending towards equilibrium conditions. The space charge effects due to semiconductor depletion of majority carriers occurs rapidly namely within time constants comparable to dielectric relaxation, provided that no deep-level traps of the GaAs are involved. During depletion condition thermal emission occurs also from the filled traps and interface states if

$$E_C - E_{Fs} \geq E_T$$

where E_T is the depth of oxide traps near the interface and interface states from the semiconductor conduction band edge there

E_{Fs} the interface Fermi level and

E_C the conduction band minimum

However, since under nonequilibrium conditions a large field exists at the interface the emission is enhanced.

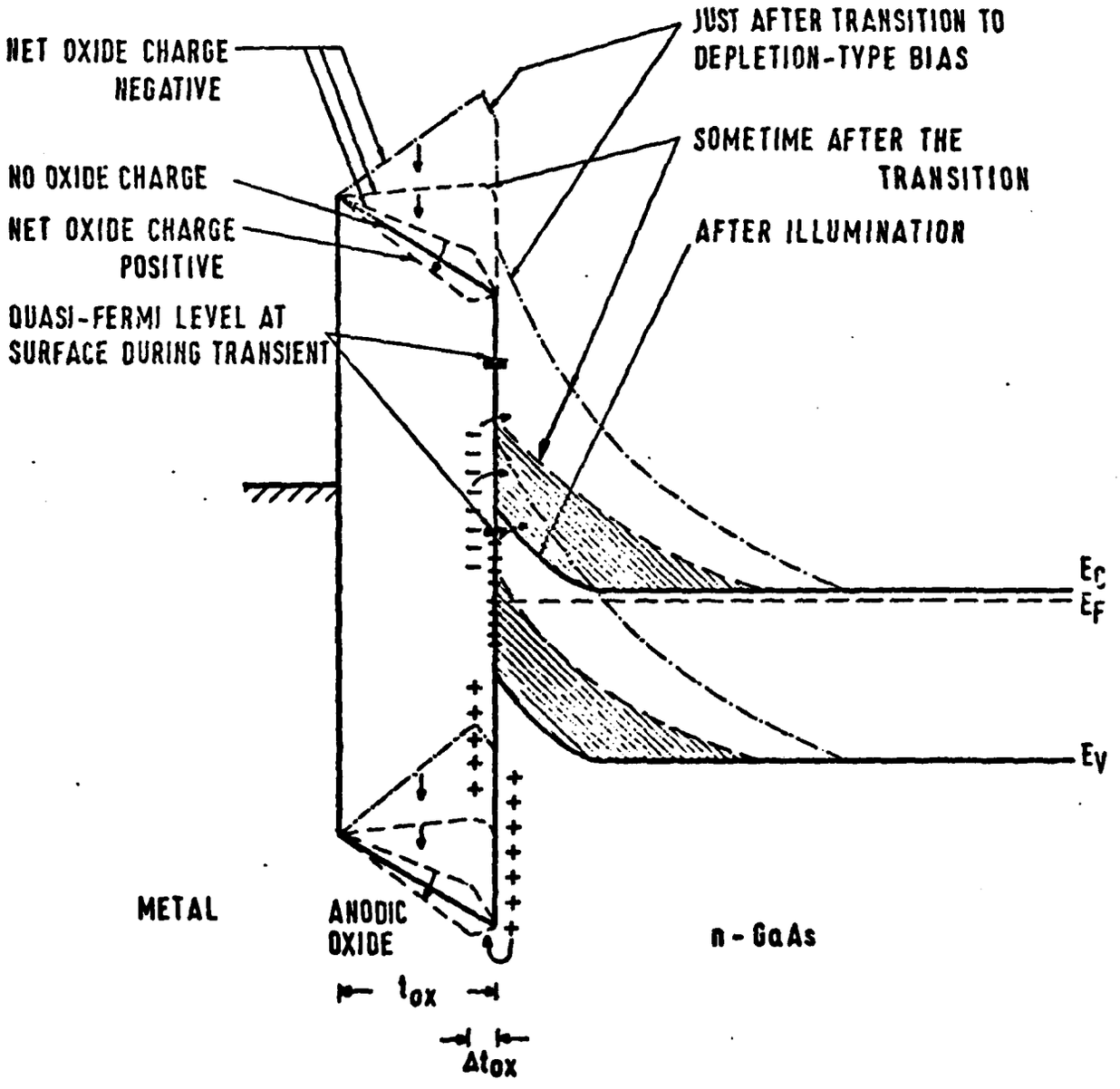


Fig. 19b Energyband diagram of n-type GaAs-anodic oxide-metal structure for pulsed bias and pulsed illumination by a Laser (λ = 632.8 nm) during depletion-type bias

The amount of charge exchange across the interface due to pulsed bias is shown in Fig. 20. As soon as an accumulation-type bias pulse is applied, the displacement current flows which occurs almost instantaneously. As the bias changes to depletion type a displacement current flows in the opposite direction but it is smaller than that for the accumulation transition because the equivalent capacitance is now reduced due to the formation of a depletion layer in GaAs. The difference between these two displacement currents appears as a slowly changing current i.e. due to the emission from the traps in the oxide as well as from the states at the interface.

Our bias consists of a periodic succession of negative and positive pulses similar to that of Schuermeyer et al.[17]. The MIS structure is illuminated for a short duration during the depletion type part of the period from a monochromatic source having energy greater than the bandgaps of GaAs (E_g = 1.4 eV). When the illumination appears, excess carriers are generated. Of these the excess majority carriers (in our case electrons) are driven towards the bulk of GaAs and the excess minority carriers (holes) are driven to and across the interface. Semiconductor band-bending is then changed as shown in Fig. 19b where the hatched area shows the amount of space charge neutralisation. The interface Fermi level shifts, however, only by a small amount.

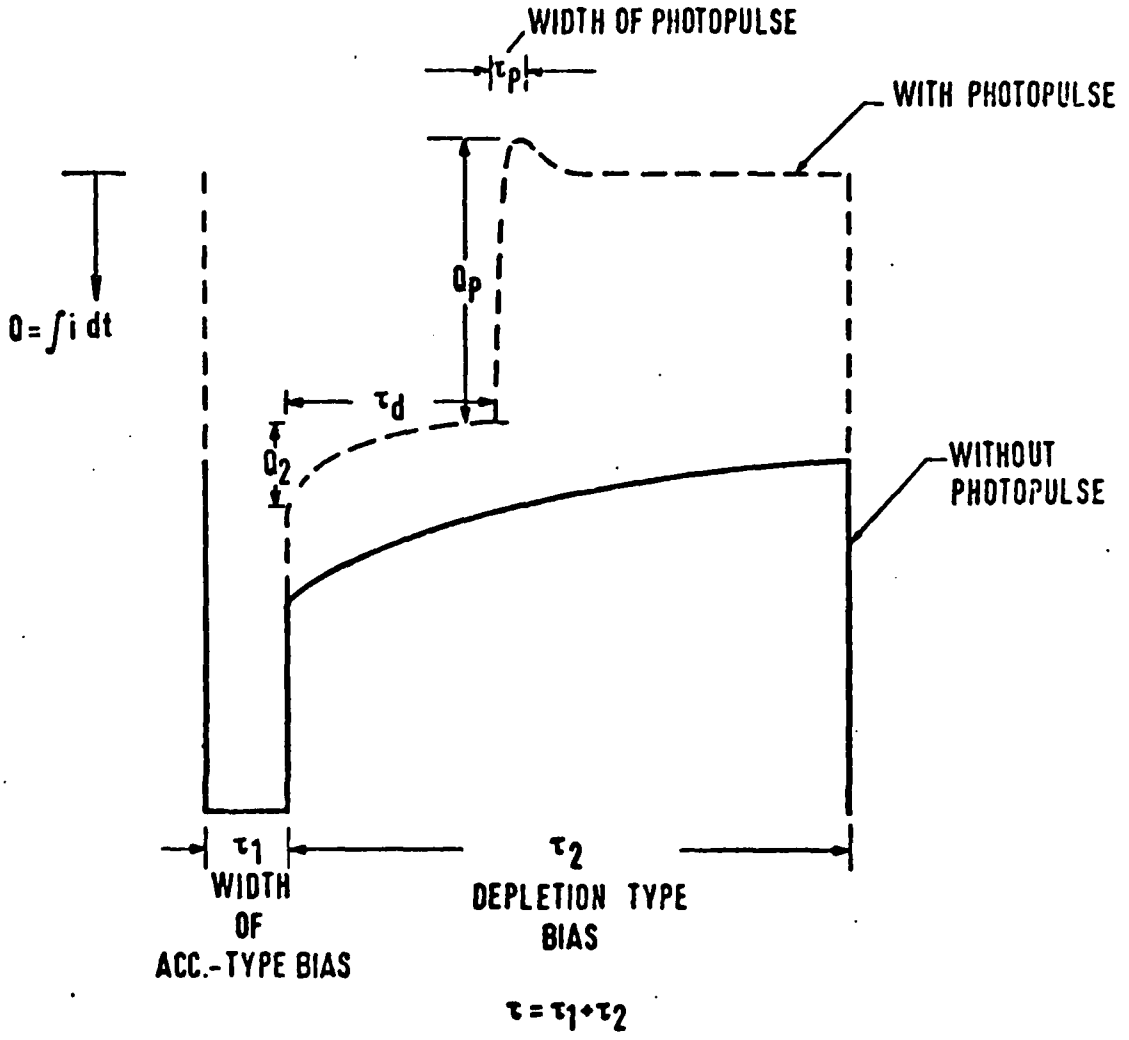


Fig. 20 Charge exchange Q (= $\int i dt$ with i the displacement current) across the interface of n-type GaAs MOS structure with anodic oxide for a bias pulse; solid-line curve is for the case when there is no illumination; the dashed line shows the charge exchange with illumination during the time τ_p

The barrier height for electrons and holes of the GaAs-anodic-oxide structure is shown in Fig. 19 where the energy for the injection of GaAs conduction-band electrons into the insulator is 2.4 eV (Yokoyama et al.[20]). As a result holes have an oxide barrier of 1.4 eV which is about the same as the bandgap for GaAs. Using a photon energy for the illumination pulse in between these two values, holes are injected from the GaAs valance band into the oxide. As they travel through the oxide, they are trapped there and possibly neutralise any electrons previously trapped at the same position. Hole trapping occurs also at the interface states. These hole traps are relatively quickly emptied when an accumulation type of bias is applied. Thus in accumulation-type bias we have electron trapping and hole detrapping and vice-versa during depletion condition. In Fig. 20 the additional charge exchange, as caused by the photo-pulse is shown by a dashed line. It is seen that for the GaAs-anodic-oxide interface faster charging occurs during the transition to accumulation but during the transition to depletion only a part of total charge flows fast and the rest comparatively slowly. However, the photoinduced charge (Q_p) transfer has 3 components. They are as follows:

i. The first component of charging consists of a rapid discharge of electrons which are trapped by the accumulation part of the pulse period and which would have been discharged only slowly in the absence of the light pulse.

ii. The second component is due to the transformation of the long depletion-type layer into only a short depletion width due to the excess carriers generated by the light pulse.

iii. The remaining component of Q_p is due to hole current flowing into the oxide and takes place only relatively slowly.

As the photopulse appears the change in potential at the semiconductor-oxide interface is capacitively coupled through the insulator capacitor to the gate electrode. Thus the photoinduced open-circuit gate potential as represented by V_p in Fig. 22 can be related to some semiconductor-oxide interface potential which includes the potential step due to oxide traps near the interface. These latter trapped charges within the oxide and at the interface cause a strongly nonuniform electric field close to the interface where thus a sharp potential step occurs which we propose here as being the reason for the large changes of V_p reported by Schuermeyer et al. [17] and presented also below.

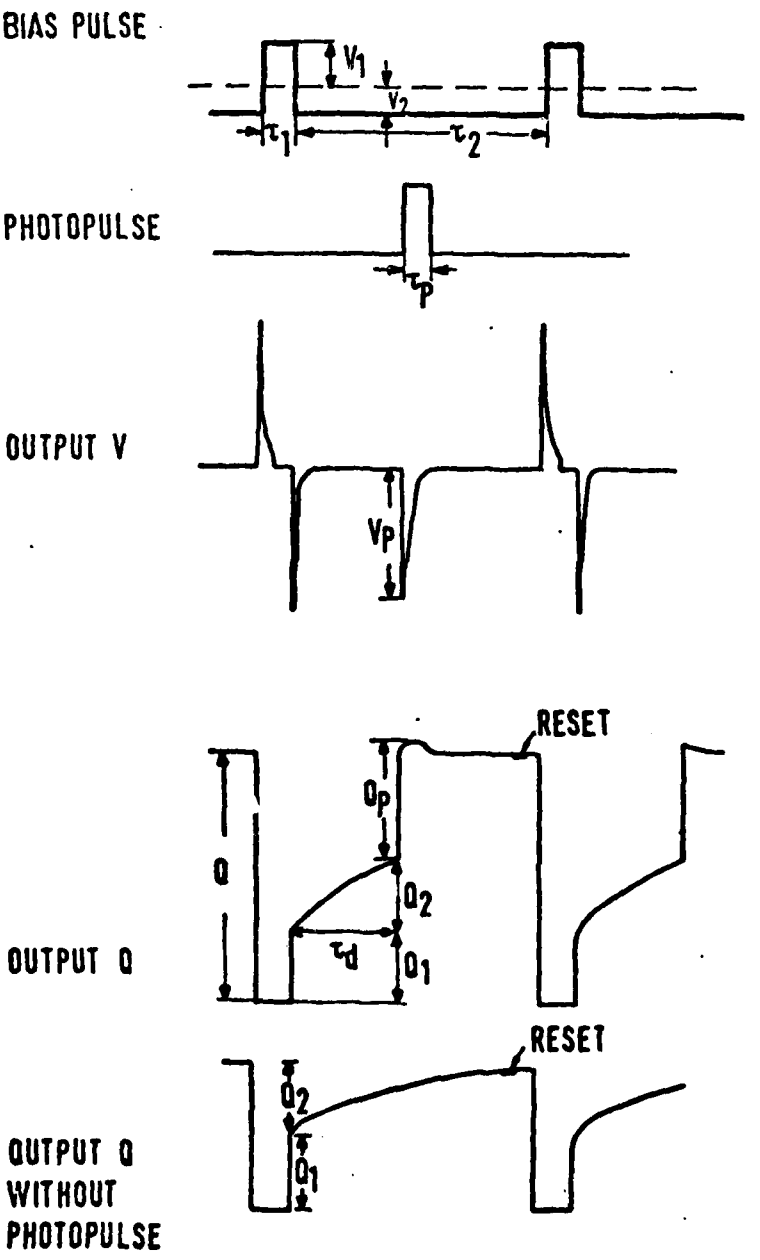


Fig. 22 Various wave forms and timing diagram

Metal-oxide-semiconductor diodes were fabricated on n-type GaAs substrates having an impurtiy concentration of $2 \cdot 10^{16}$ cm^{-3}. The native oxide on GaAs was grown by the method as described by Bayraktaroglu et al [21]. The thickness of the oxides was in the range of 1300 - 1900 Å as determined from C-V measurements and from the overpotential developed during anodisation. Front side illumination was used and for this purpose the gate electrode was made to be very thin, namely for aluminium and gold contacts, 150 Å and 90 Å respectively. Illumination was achieved by Helium-Neon-Laser having a wavelength of 6328 Å corresponding to $h\nu = 1.96$ eV. After fabrication, the devices were tested by C-V and I-V measurements. The area of the diodes was 0.8 mm^2 and the leakage current was in the range of a few nanoamp/cm^2 for a few volts.

The measurement of the photo-induced open-circuit voltage V_p and of the photo-induced charge Q_p was performed by a measuring set-up as illustrated in Fig. 21. A mechanical chopper was used which was synchronised by the bias pulse frequencies. By using appropriate delays it was possible to place the photo-pulse at any position within the bias pulse period. V_p was picked up by a high-input-impedance amplifier and Q_p was obtained from a charge integrator. It was necessary to reset the integrator for every cycle and this was done towards the end of the depletion-bias part. The measurement of V_p requires some degree of judgement and hence R_s

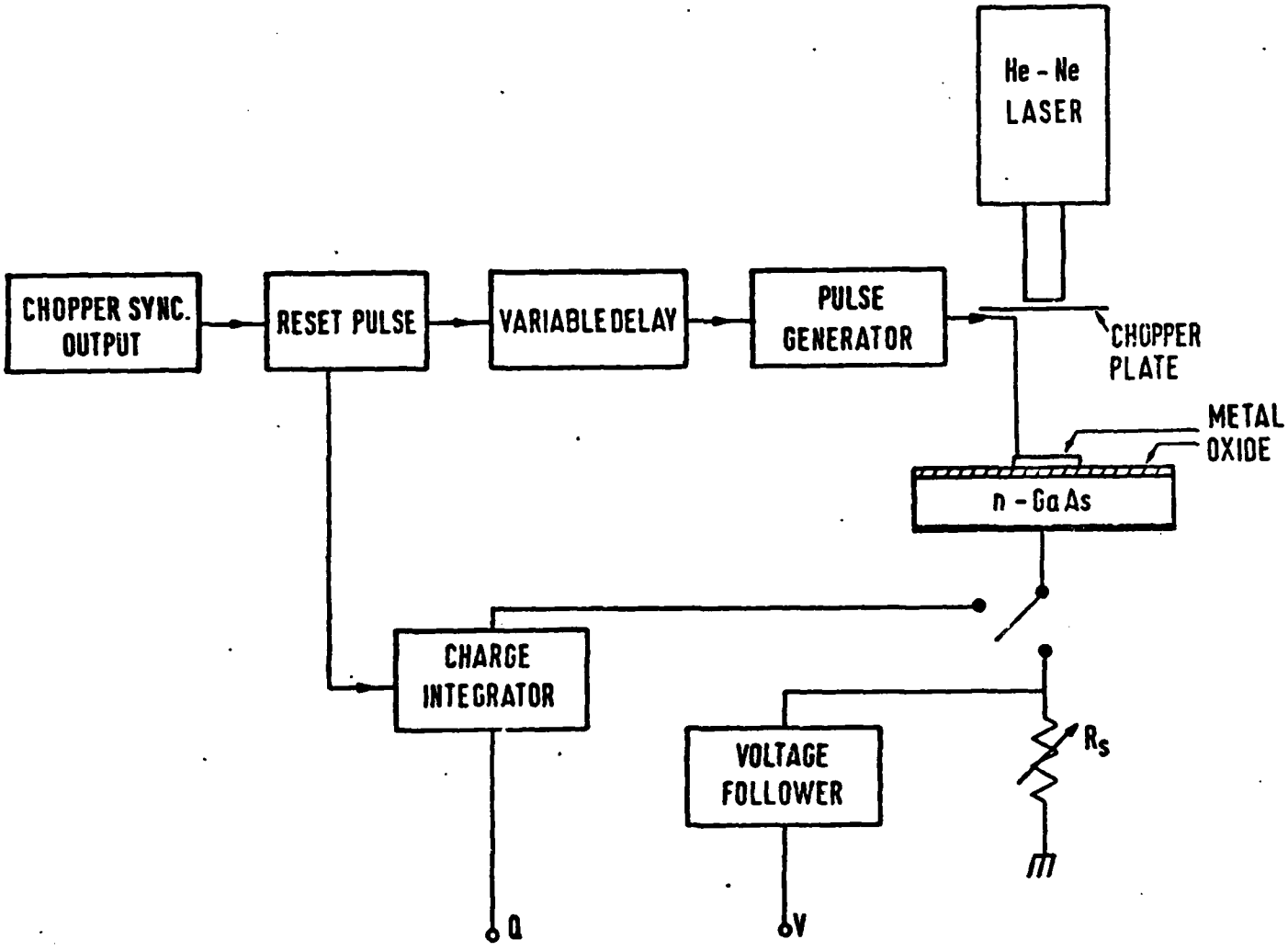
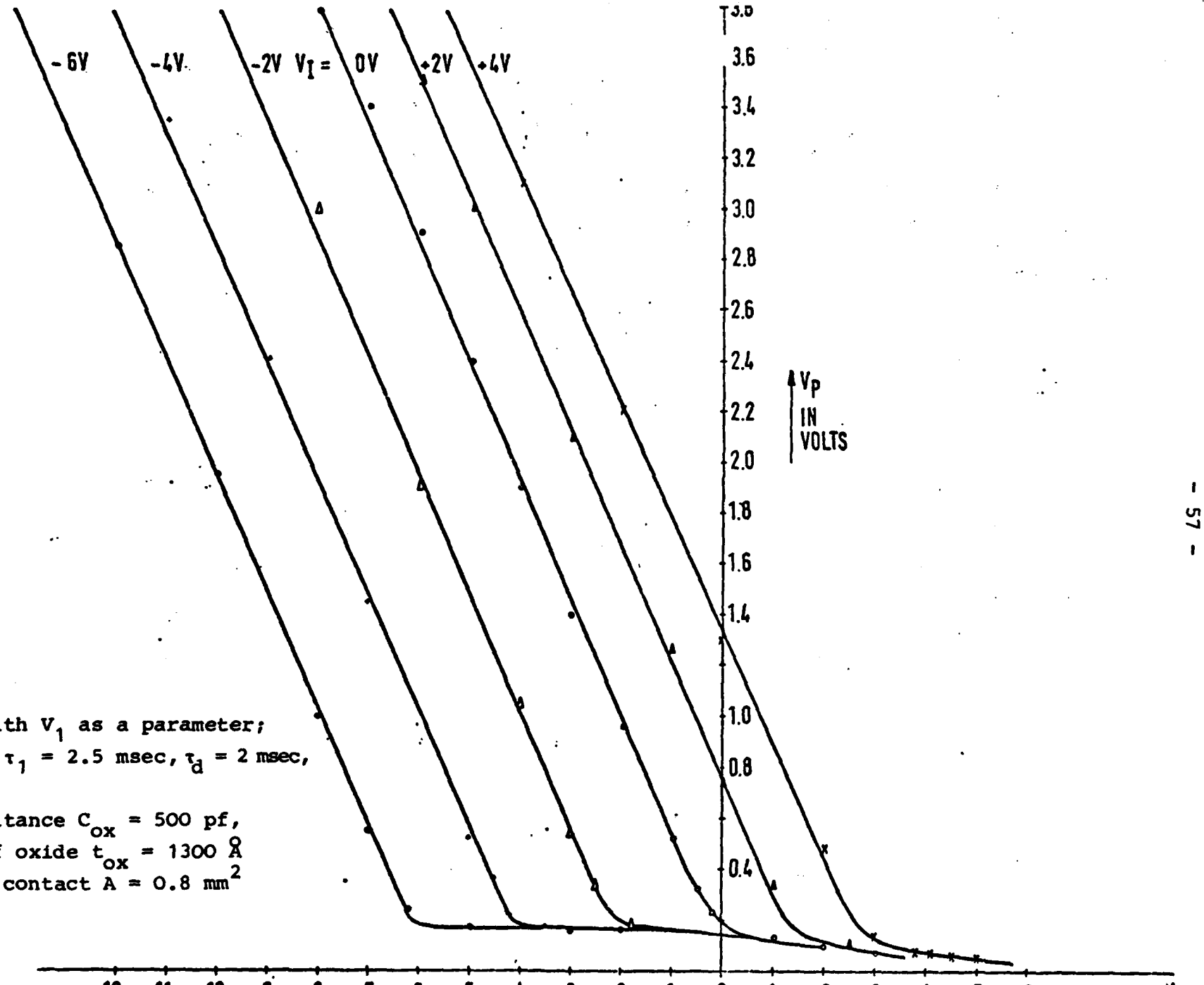


Fig. 21 The measuring set-up for the range of bias-pulse frequency 10 - 120 Hz

has to be varied so as to obtain a maximum peak of V_p. In all cases the bias-pulse rise time and fall time were in the range of a fraction of a microsec.

The photo-induced pulse V_p is plotted as a function of bias V_2 in Fig. 23 where V_2 is varied from accumulation to depletion type bias. The different curves are for different accumulation type of bias V_1 and the frequency of the bias pulse is 120 Hz. The diode is illuminated at the middle of the time of V_2 and the waveforms of V_p and Q_p are given in Fig. 22. It is observed that increasing the bias pulse amplitude causes an increase of V_p. A change of offset bias has very little effect upon V_p except that the discharge is a little faster with increasing depletion-type of offset. With the change of V_1 the curves are shifted in parallel and the slope is almost constant. The surface potential cannot be inverted as it is evident from the lower portion of the curve in Fig. 23 which is almost flat and does not cross the X-axis. The curve shows two distinct regions, the lower portion being flat and the upper part changing steeply. The lower portion is obtained, when $V_2 > V_1$ i.e. the MIS structure is in an accumulation-type region. Since in accumulation-type bias a very small space-charge layer is present, the photopulse response is limited to 0.2 V. When $V_2 < V_1$ the MIS structure is driven to deep depletion conditions, most of the applied voltage pulse amplitude occurs across the depletion region as the oxide potential distribution only changes slowly. The photopulse - generated carriers then neutralise a portion of the space charge. An increasing pulse amplitude results therefore in an increase of the photopulse voltage V_p. Development of any space charge layer in



V_p vs. V_2 with V_1 as a parameter;
τ = 8 msec, τ_1 = 2.5 msec, τ_d = 2 msec,
$\tau_p = \tau/20$,
oxide capacitance C_{ox} = 500 pf,
thickness of oxide t_{ox} = 1300 Å
and area of contact A = 0.8 mm^2

Fig. 23

GaAs can take place within the pulse time constants, so that a change in pulse amplitude is followed immediately by the space charge layer in the GaAs which thus behaves like a one-sided step junction. The amount of charge in such a layer depends upon the square root of the potential applied across it. Therefore V_p should behave similarly to the charge-voltage relation. However, due to the presence of traps, being filled and emptied, a different behaviour of V_p is observed. Keeping the bias - pulse amplitude constant, the occurence of the photopulse at different times of the bias period would indicate a change in V_p related to the process of trapping and detrapping.

The amount of charge flow across the interface during one cycle is shown in Fig. 20 in which Q_p is caused by the photopulse. Without any illumination the discharge is slow and is almost complete during V_2 when the frequency is about 10 Hz. It is certain that the photopulse causes some of the traps in the oxide (and in GaAs) as well as the interface states to emit electrons. The discharge-time constant of interface states is much smaller than the time allowed for the discharge of traps. The width of the photo-pulse is very short to cause complete detrapping of carriers. But using a low frequency of bias pulses which in turn causes proportionate increases in width of the photo-pulse, hole trapping is also effected and this is evident later in this report.

When the width of the photopulse is short, the ratio Q_p/V_p should be approximately the oxide capacitance. This can therefore be obtained from the plot of Q_p vs. V_p. It is observed that this plot is a straight line confirming to a certain extent that the slope is a measure of the capacitance of the oxide. This has been checked for various amplitudes of bias pulses and has been confirmed also by Schuermeyer et al [17]. But the ratio we then obtained is about 100 pf greater than the true oxide capacitance, which has been determined independently by the extrapolation of the asymptotic accumulation-bias capacitance. Since the frequency range of operation is 12 to 120 Hz, we observed oxide traps. Therefore, we attribute this excess capacitance to the capacitance arising from the trapping effect in the oxide near to the interface which actually reduces the effective thickness of the dielectric. This excess capacitance can be placed in parallel to C_{ox} in the equivalent circuit. Under illumination, when the semiconductor band is flat except immediately near the interface, the capacitance due to interface states will be in series with C_{ox}. Since the ratio Q_p/V_p is always somewhat greater than C_{ox}, it is obvious that oxide trapping charges are important. The ratio Q_p/V_p bears actually much information and its dependence on the frequency of light chopping is complicated. An adequate theoretical analysis is necessary to obtain an insight into this quantity. The calculated charge density from the excess capacitance of the ratio Q_p/V_p is of the order of 10^{11} cm^{-2}. However, the total density of traps can be expected to be even higher than the number of carriers captured in our time constants.

The charging and discharging behaviour of the traps has been illustrated in Fig. 24, 25, 26 and 27. In Fig. 24 V_p is presented against the logarithm of τ_1. In Fig. 24a the photopulse was placed at the end of τ_2. The increase of τ_1 is then accompanied by a reduction of τ_d. It is seen that V_p increases logarithmically. Increasing τ_1 beyond a few millisecs causes slower increases in the filling of traps but a more pronounced effect is that a reduction of the discharging time causes these charges to be accumulated at the levels of the traps and the interface states. As a result, both the quantities Q_p and V_p increase. But the nature of these variations has to be more critically studied and should be related to the process through which traps are filled by injection and emptied by the process of emission. In Fig. 24b τ_1 was increased from 1 μ sec to a few millisec, keeping τ_d, the discharge time before the appearance of the photopulse, constant. It is noticeable that both at 13 Hz and 125 Hz V_p increases almost linearly with logarithm of τ_1 over 2 decades. Beyond this linear range V_p changes slowly. Increasing τ_1 up to 50 msec no saturation is observed but goes on increasing rather slowly. However it is observed that for a smaller pulse width τ_1 (in the μ sec range) the ratio Q_p/V_p yields a very large value, being far away from the actual insulator capacitance. Therefore it seems that a low value of τ_1 the high non equilibrium condition of traps or states filling prevent Q_p/V_p to be used directly as a measure of insulator capacitance.

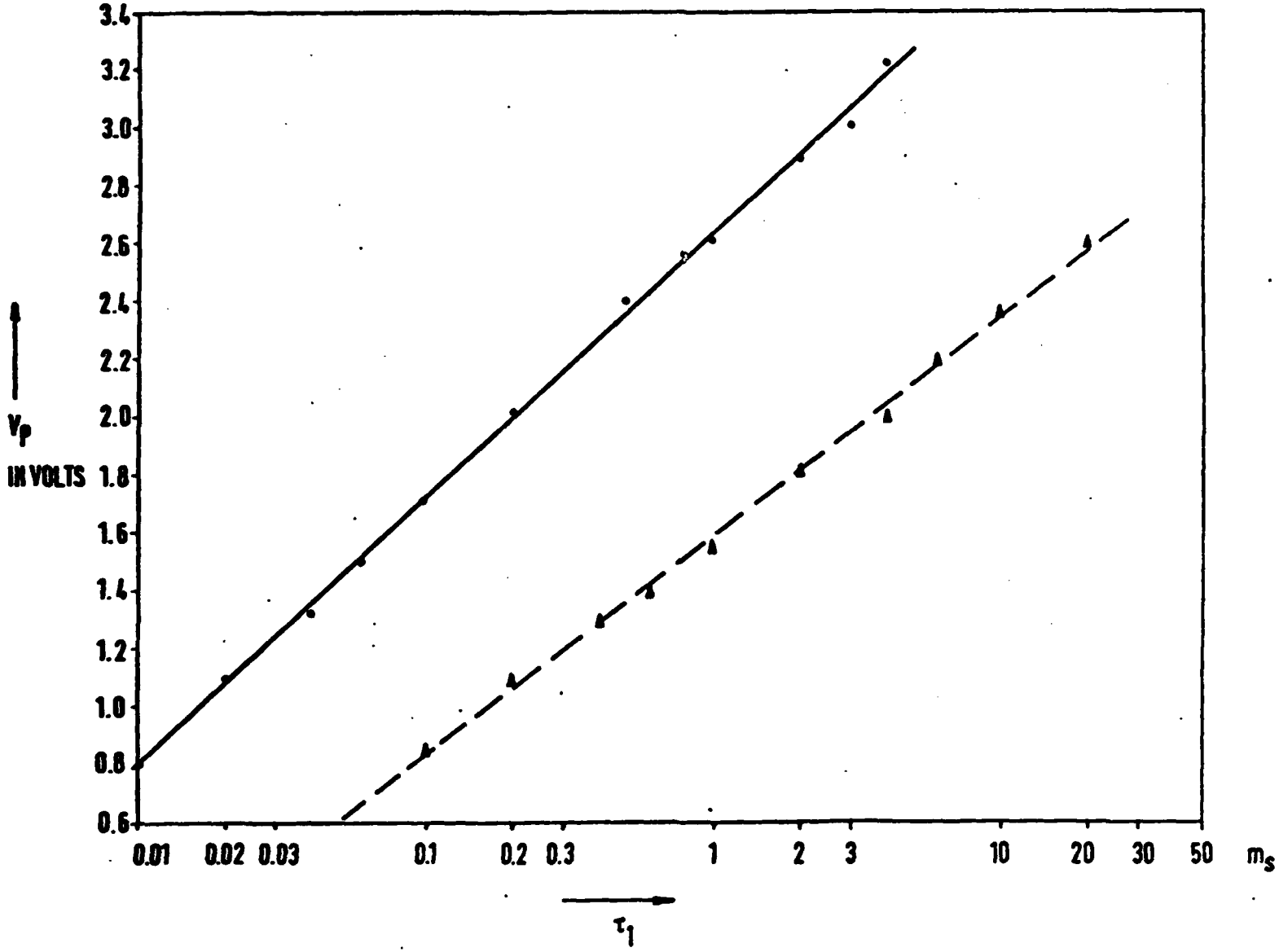


Fig. 24a V_p vs. τ_1 at τ = 8 msec as shown by solid line and at τ = 72 msec as shown by dashed line; the photopulse is locadted towards the end of τ_2. The increase in τ_1 is accompanied with decrease in τ_d, V_1 = 5 V, V_2 = - 3 V, C_{ox} = 445 pf, t_{ox} = 1450° A and A = 0.8 mm^2

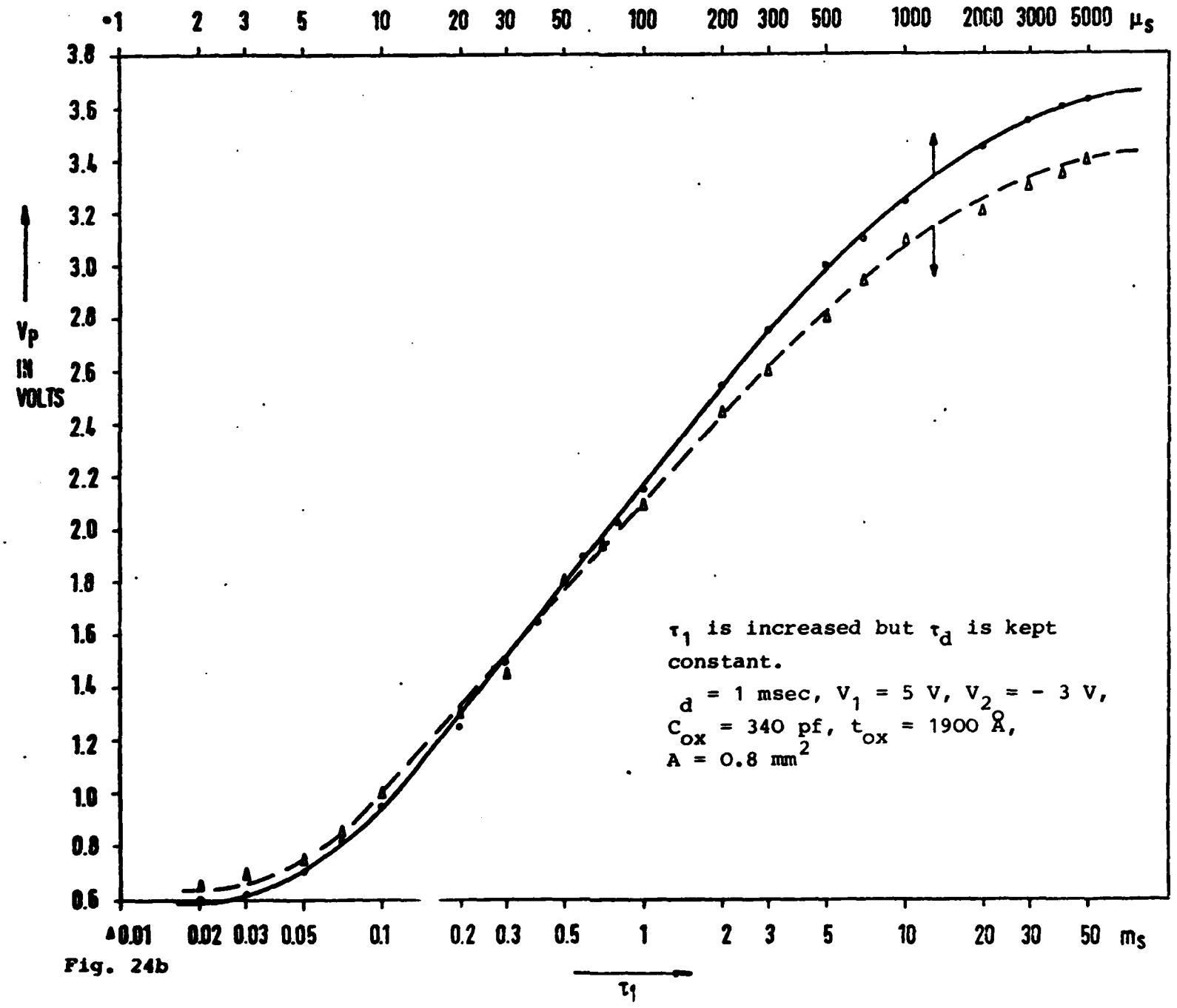

•1 2 3 5 10 20 30 50 100 200 300 500 1000 2000 3000 5000 μs
3.8
3.6
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
VP IN VOLTS
0.01 0.02 0.03 0.05 0.1 0.2 0.3 0.5 1 2 3 5 10 20 30 50 ms
τ1
τ1 is increased but τd is kept constant.
d = 1 msec, V1 = 5 V, V2 = - 3 V,
Cox = 340 pf, tox = 1900 Å,
A = 0.8 mm2

Fig. 24b

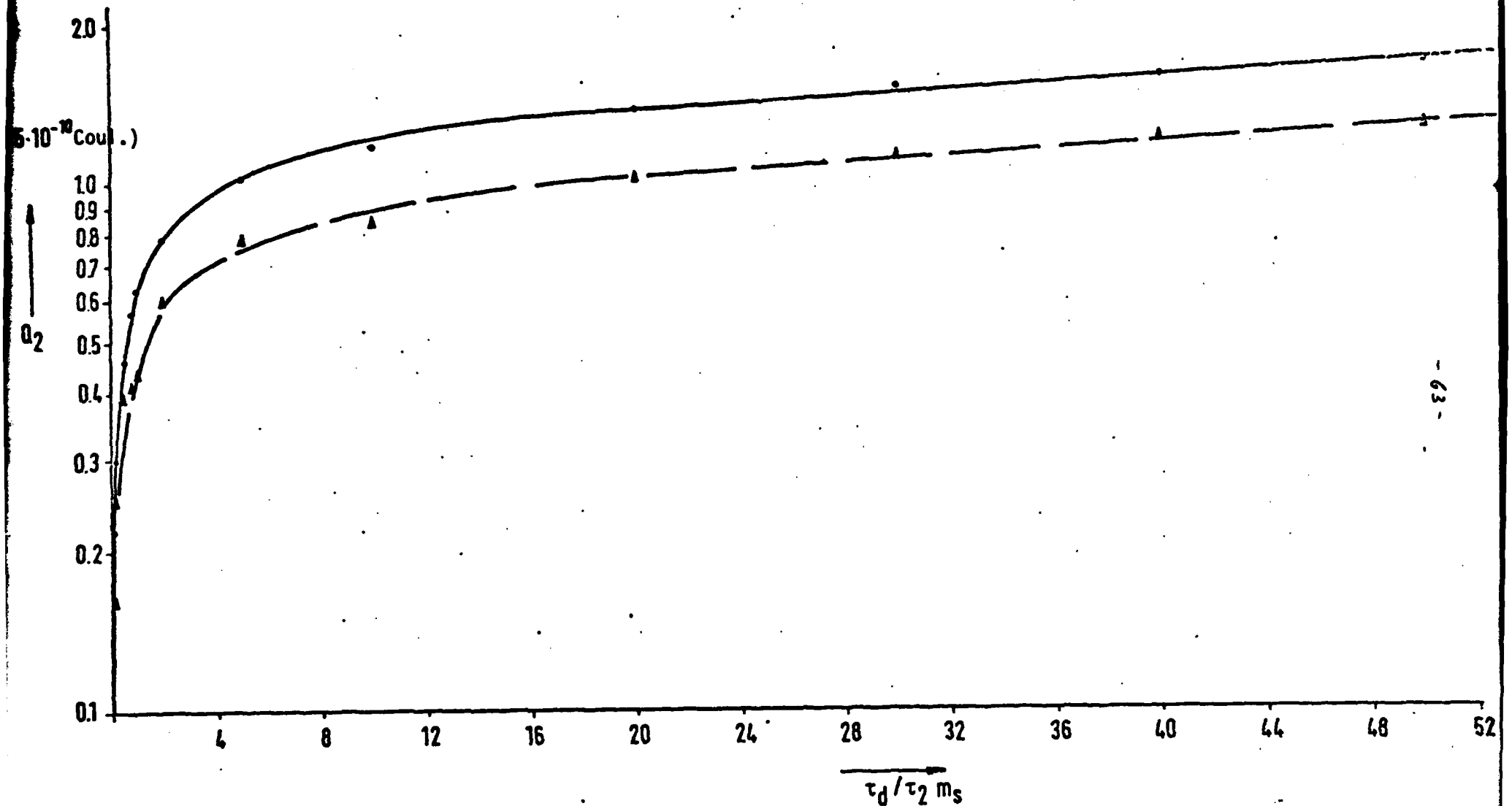
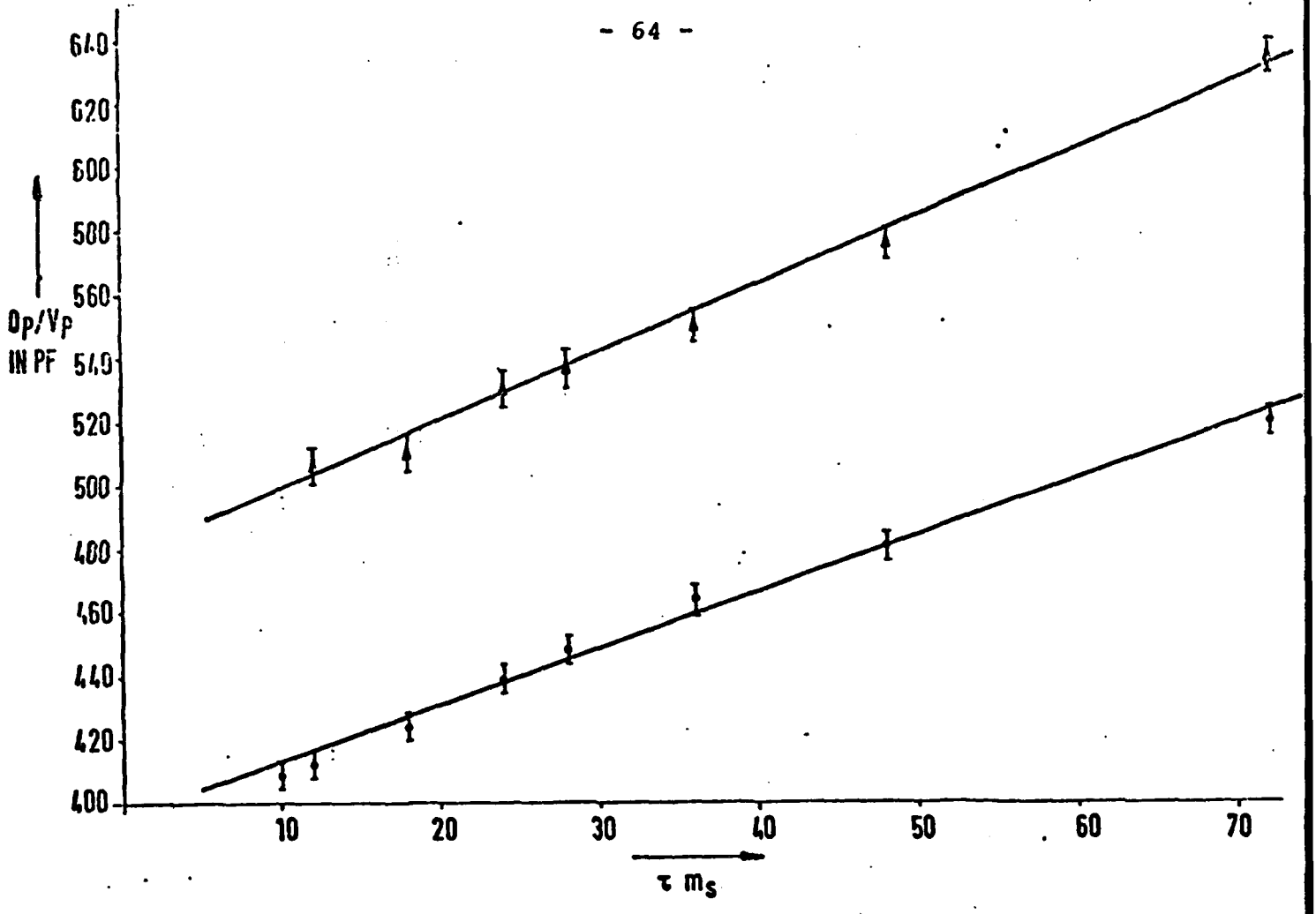
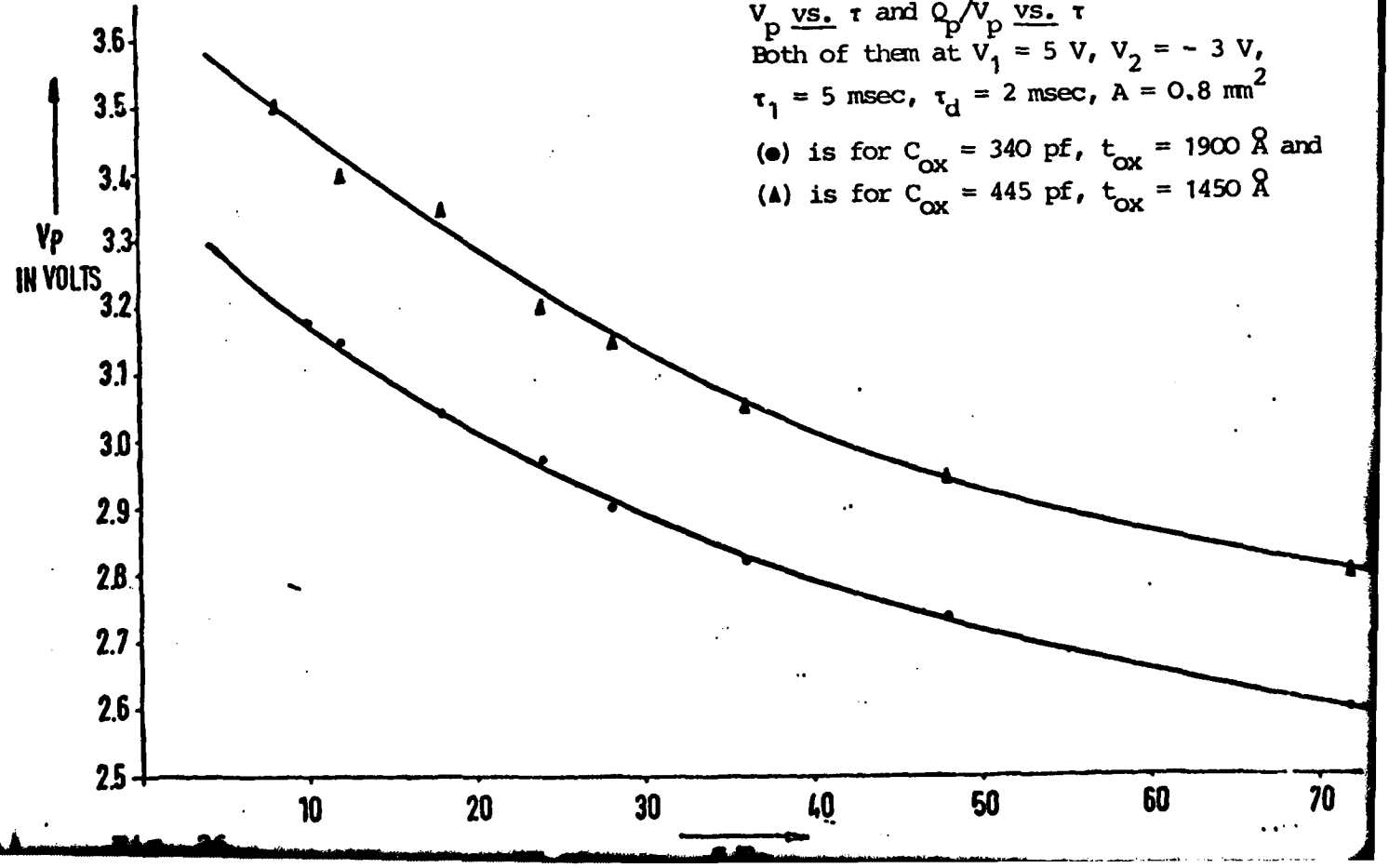


Fig. 25 Q_2 vs. τ_d as shown by solid line is with photopulse and Q_2 vs. τ_2 as shown by dashed line is without illumination; the position of photopulse being fixed towards the end of τ_2; $V_1 = 5$ V, $V_2 = -3$ V, $\tau = 72$ msec, $\tau_1 = 2$ msec, $C_{ox} = 340$ pf, $t_{ox} = 1900$ Å and $A = 0.8$ mm^2





V_p vs. τ and Q_p/V_p vs. τ
Both of them at V_1 = 5 V, V_2 = - 3 V,
τ_1 = 5 msec, τ_d = 2 msec, A = 0.8 mm^2
(●) is for C_{ox} = 340 pf, t_{ox} = 1900 Å and
(▲) is for C_{ox} = 445 pf, t_{ox} = 1450 Å

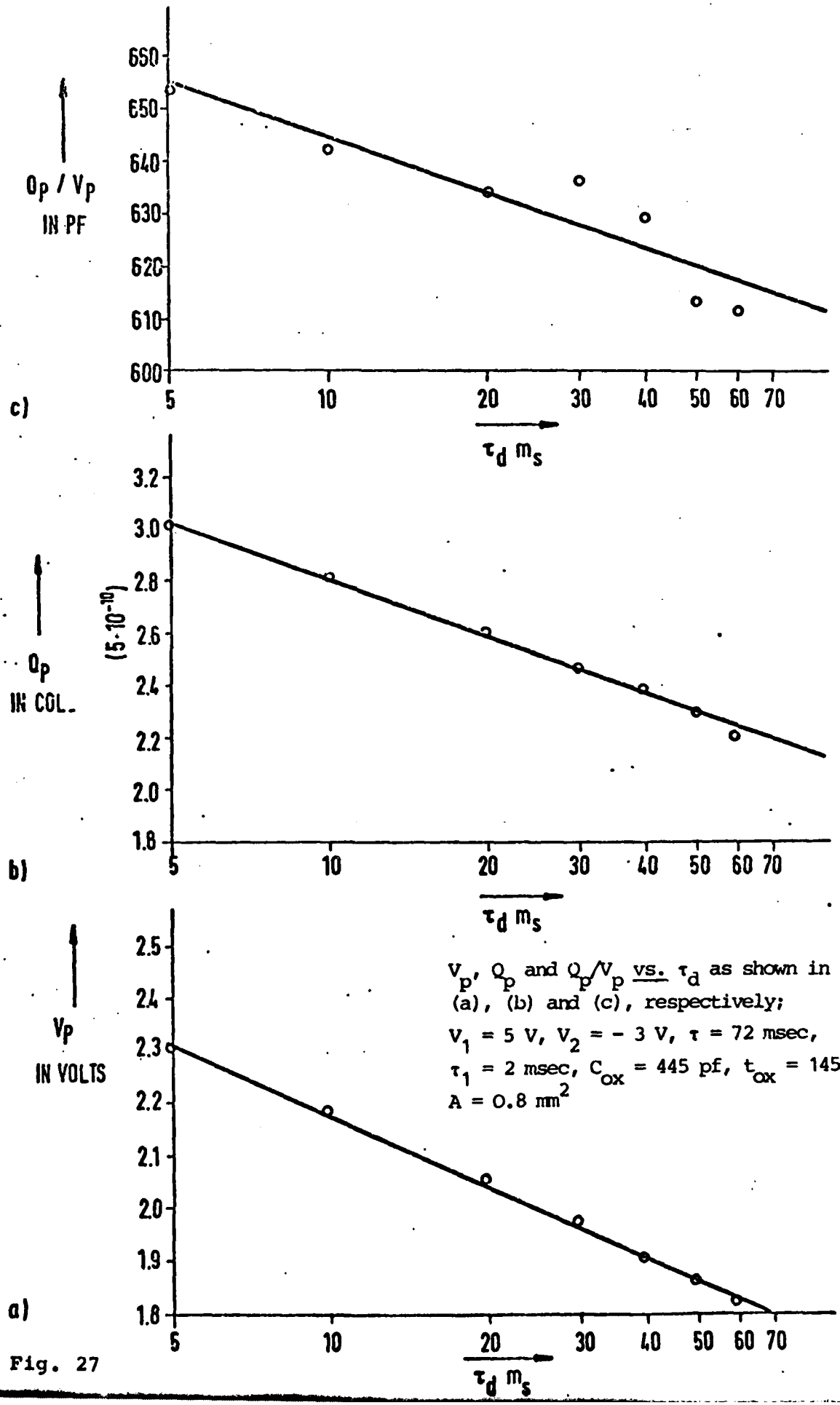


Fig. 27

V_p, Q_p and Q_p/V_p vs. τ_d as shown in (a), (b) and (c), respectively;
$V_1 = 5$ V, $V_2 = -3$ V, $\tau = 72$ msec,
$\tau_1 = 2$ msec, $C_{ox} = 445$ pf, $t_{ox} = 1450$ Å,
$A = 0.8$ mm^2

Applying pulses of higher amplitude that is driving the MIS structure deep into accumulation causes, further filling of traps. The total charge transfer across the interface can directly be found from the Q dependence shown in Fig. 20 and 22 in which Q_1, Q_2 and Q_p are the normal displacement charges, the normal discharge without any illumination and the discharge due to illumination respectively. With a steady illumination faster and increased discharge is observed. An increase of bias-pulse amplitude causes all the components of Q to increase. The charge Q_2 is actually caused by a discharge from the levels of the traps and the interface states and the increase of Q_2 was found not to saturate until breakdown. With pulses of about 30 volts of amplitude for a MIS structure having an oxide thickness of 1300 Å, the trap density was found to be above $5 \cdot 10^{12}$ cm^{-2} and this condition cannot exist for a longer time because breakdown occurs. With an increase in the amount of trap filling the rate of discharge is also found to increase.

Applying the photopulse towards the end of τ_2, the discharge during τ_d is found to be neither exponential nor logarithmic in time. But after τ_d = 10 msec, it varies almost exponentially, as is shown in Fig. 25.

In Fig. 26 V_p and the ratio Q_p/V_p have been plotted as a function of the time period of pulsed bias τ. The ratio Q_p/V_p is of interest because it can be used to evaluate the capacitance due to the oxide of the MIS system. The bias pulse width and

the delay in the appearance of the photo-pulse within the depletion bias time τ_2 have been kept constant. But a change of τ is accompanied with a change of photo-pulse width τ_p which is equal to $\tau/20$. It is clear that with an increase in τ, V_p decreases monotonically as is observed in Fig. 26 , but the ratio of Q_p/V_p increases linearly with τ. This effect is explained as a hole charging process. During depletion bias the excess minority carriers are drifting towards the interface and the majority carriers towards the bulk of the GaAs and thus hole trapping occurs because they receive energies greater than barrier at the interface, from the illuminating photons. This causes the magnitude of V_p to decrease. As previously said, the ratio Q_p/V_p is evaluated as a capacitive quantity due to charging the capacitance by minority carriers. But during photo-excitation holes are captured by the trap levels within the oxide near the interface with the semiconductor and result in an increased capacitance as defined from the ratio of Q_p/V_p. The density of trapped holes can be calculated as follows

$$Q_p = \Delta C\ V_g + C_{ox}\ V_p$$

where ΔC is the excess capacitance due to hole trapping and

$$\Delta C = \frac{(Q_p/V_p) - C_{ox}}{V_g/V_p}$$

Thus an increase in capacitance (of 200 pf) due to hole trapping gives a density of trapped holes of about $5 \cdot 10^{11}$ cm^{-2}. These holes enter into the oxide and are trapped, thus also neutralising any electrons still trapped in the oxide.

In Fig. 27 V_p, Q_p and Q_p/V_p have been plotted against the discharge time τ_d before the appearance of the photopulse. It is seen that both V_p and Q_p decrease linearly along the log-time scale whereas the decrease in the ratio Q_p/V_p with log-time is not strictly linear. Shifting the photopulse i.e. increasing τ_d, causes the discharge time of trapped electrons to increase, and consequently V_p decreases. The same effect is found in Fig. 24a. When τ is longer e.g. in the range of secs., V_p reduces to values ranging from about 0.1 to 0.2 volt, which is the response due to steady state bias. In this case τ_1 was about 2 millisecs, which means that injection is not complete at a pulse amplitude of 8 V. The ratio Q_p/V_p shows a little decrease which is due to electron detrapping as caused by depletion bias. However, it is expected that with a heavy injection bias voltage close to breakdown, this ratio changes significantly because a large amount of trapped electrons in the oxide create some local conduction area.

So far we have observed that both charging and discharging of the native oxide have a logarithmic time dependence. This has been previously reported by Kohn and Hartnagel [22] but they have referred this only to the injection process. It is certain that a leakage current component does not affect our results noticeably because it was found to be in the range smaller than 1 nA for an applied voltage of 12 volts. Thus there remains three processes which may be involved. They are thermal emission, a tunnel current and the photo-ionisation component. Photo-ionisation of the traps

have been neglected so far in our discussion here, but would have to be included in an improved analysis. It has to be assumed, however, that both thermal and field emission have a strong effect on the experimental behaviour, one being predominant over the other depending on the frequency. It is generally accepted that emission causing the discharge is a thermal process and the energy of the state levels can be found from the plot of time-constants vs. 1/temperature and that the slope gives the activation energy. Since the barriers at the semiconductor interface is small, the charging of the oxide depends during the injection time upon interface state traps arising due to defect levels introduced in the oxide during the anodisation process. In order to observe the discharge for a longer time we had to decrease the frequency but this resulted in an increase in τ_p, adding hole trapping during the time of electron emission. However, it is quite convincing that the discharge has at least a tunnelling component affected by illumination in addition to the thermal one. Thus superimposition of the two processes causes the picture to be complicated. Recently it has been shown by Yamabe et al [23] that the discharge of avalanche trapped electrons in SiO_2 on Si is also due to a tunnelling phenomenon. Therefore we can consider also in our case that field emission occurs because of an increase of field at the surface as caused by illumination.

The results so far obtained are only in a narrow range of frequency of pulsing. It is necessary to observe the discharging down to 0.1 Hz. It is expected that a response from deep interface states and traps can be found when the frequency is lower than one Herz. So further work is to be continued to include those factors which have not been considered.

CHAPTER V

Conclusions and Recommendations

After various experimental results, both by some of the present authors as well as by workers from other research centers, have lead to the understanding that native oxides on GaAs have a wide and complex interface region with strongly electrically active states and traps, due to the different oxidation rates of Ga and As, efforts were undertaken here to use Al_2O_3 with a semiconductor-oxide interface of carefully prepared composition. Since it is also known that the deposition of any non-native material, both insulating or metallic, produces a non-stoichiometric surface layer of GaAs, both an enhancement of Ga and the use of GaN as thin surface region were employed. The latter scheme was also particularly selected because there are suggestions that oxides on GaAs might always lead to a very high density of active interface states. As could be shown by Chapter 2, all these efforts gave capacitance-voltage characteristics which can be explained by the pronounced effects of interface states and traps, using the model of a previous co-worker[2], although often some promising features of reduced dispersion for accumulation-type bias and of a low-frequency inversion-type capacitance appearing already with 10 - 100 Hz. In view of these many, little convincing improvements, and also due to a lack of time and funding, no inversion-type MOSFETs were developed as would be needed to clearly demonstrate at microwave frequencies the existense of a mobile inversion-layer

charge (the capability for this FET manufacturing is, however, available as can be seen from the depletion-type MISFETs produced in the past). We are convinced thus that a relatively straight-forward passivation method for GaAs is unlikely and that efforts should now be made first to study primarily the various microreactions between GaAs and any film deposited by various means, as possible with ESCA, Rutherford backscattering and other techniques. The intention of the authors is now indeed to become even more strongly involved in such an effort than hitherto, where the combined UHV-ESCA and ISS system here will be very valuable.

In order to explore the charging and discharging effects in the interface layer more fully, and to propose a more refined model for the presently achievable MOS devices, a previously developed photopulse method was extended by incorporating a monochromatic laser pulse. In this way not only electron-hole pairs are produced in the depletion layer for a neutralization of this layer by the photogenerated minority-carrier accumulation, but also some of the carriers can be lifted across given energy barriers, such as hole transfer into the insulator. These efforts, which are reported in Chapter 4 demonstrate that a relatively wide charge-trapping layer exists at the interface. The corresponding model proposed allows then to interpret by a Fermi-level pinning concept many of the previously published results which seemed to show that the Fermi-level has become mobile at the

interface due to a particular technology. This model is based on substantial charge trapping in an interface layer of around 100 Å so that, even with a fixed Fermi level at the oxide-semiconductor interface, a capacitance and charging behaviour is possible which can give the impression of a movable Fermi level.

The efforts of electroluminescence were continued an lead to evidence that the emission efficiency depends on the quality of the GaAs surface underneath either a thin oxide or a metal. Also these results point now to the need for further microreaction studies of the GaAs surface with any film deposited on it.

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Dr. Marc Faktor of the British Telecom, Research Laboratories in Martlesham Heath, Ipswich, is thanked for discussions and arrangements for the Auger data of Chapter 2 to be made at his laboratory on our samples.

Many of our students are to be mentioned here too, who contributed through their projects with us to obtain some of the results reviewed here, which were selected from the substantially larger amount of new data found through these efforts. Their names together with the thesis titles are given in Appendix II.

Finally Mr. Alam is thanked for his contributions to this work during his sabbatical leave from his Technical University of Dacca in Bangladesh.

Appendix I shows by the papers published during the report period together with the various authors who were involved in the main parts of this work.

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"Darstellung der Halbleiterbauelemente zur Frequenzvervielfachung im GHz-Bereich und Diskussion der entsprechenden Schaltungen (Literaturarbeit)"